TOSHIBA
Leading Innovation

Toshiba UFS Memory Overview for LGMC

in Seoul, Korea
Oct. 22nd 2015

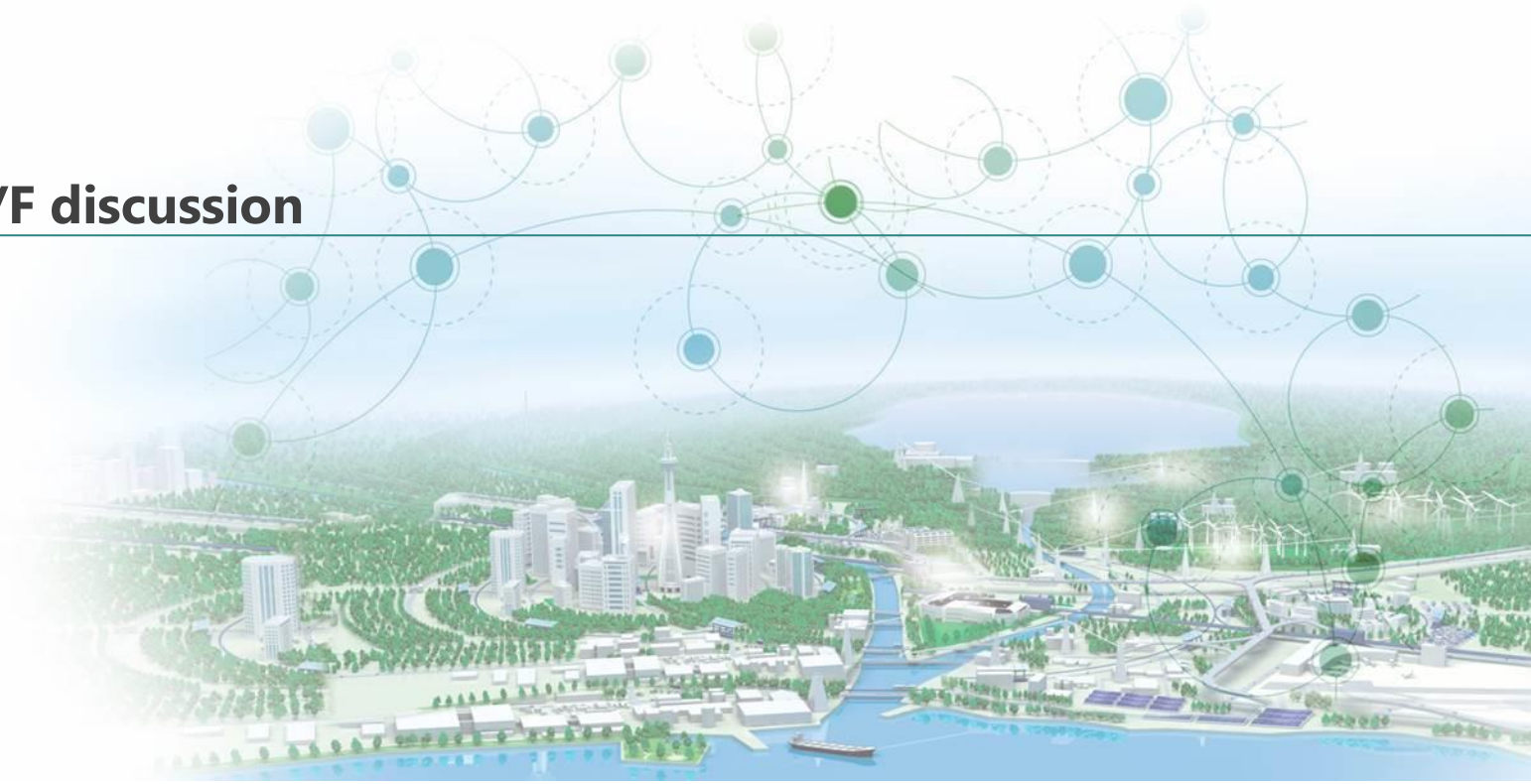
Memory Application Engineering Dept. I
Memory Division
Semiconductor & Storage Products Company
Toshiba Corporation

e•MMC™ is a trademark and a product category for a class of embedded memory products built to the joint JEDEC/MultiMediaCard Association (MMCA) MMC Standard specification.

Agenda

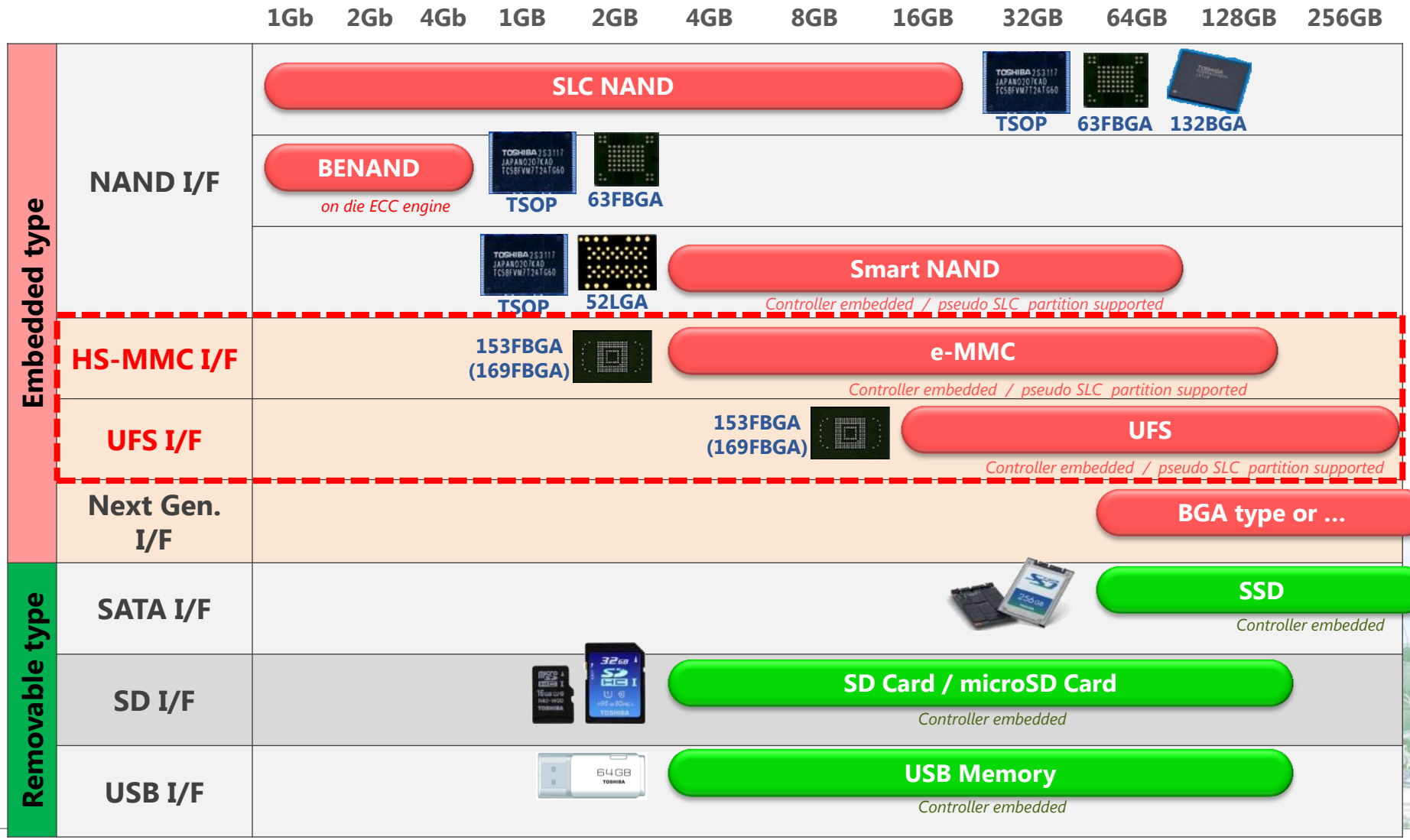
- Comparison : UFS vs. e-MMC
- UFS Specific feature : UME (Unified Memory Extension)
- Toshiba UFS latest roadmap

Memory I/F discussion



Toshiba's Current Portfolio

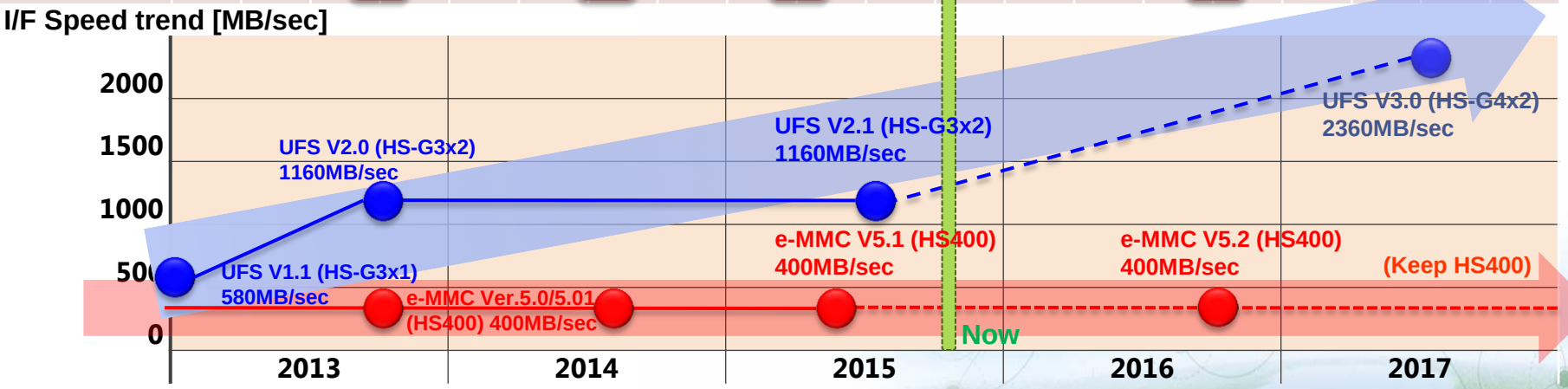
e-MMC is a DeFact Standard Memory for Mobile Applications such as Smartphone and Tablet. UFS is a successor of e-MMC.



JEDEC / MIPI standardization schedule

Toshiba has essential IP's (M-PHY, UniPro, NAND, Controller) for UFS development. We will expand and lead UFS memory market with these.

Standard Publication	2013				2014				2015				2016				2017			
	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q
M-PHY			3.0 HS-G3								4.0 HS-G4									
UniPro			1.6								1.8								HS-G4x2lane? New topology?	
UFS			2.0 HS-G3x2lane										2.1 FFU / Others				3.0			
e-MMC			5.0				5.01			5.1					5.2					



Toshiba's strategy
e-MMC : Keep supporting the customers, but no huge investment anymore.
UFS : Focusing on UFS development and following JEDEC standard and market.

New feature list for each standard ver.

Toshiba has essential IP's (M-PHY, UniPro, NAND, Controller) for UFS development. And move the development resource to UFS step-by-step.

e-MMC			
Ver.	**5.0/5.01**	**5.1**	**5.2**
Standard	**JESD84-B50 / 50.1**	**JESD84-B51**	**tbd**
Publication	**Sep.'13 / Jul.'14 (Done)**	**Feb.'15**	**3Q'16(Not fixed yet)**
Main New feature on consensus list	HS400 & Adding DS pin Product State Awareness Device Health Report Field FW update etc.	Command Queuing (Optional) Cache barrier RPMB Throughput Improvement(8KB) Enhanced Strobe at HS400 etc.	tbd Companies don't like to introduce the items which causes HW changes.
Main Proposal Under discussion	n/a	No other Proposal (Fixed in Dec.'14 Committee meeting)	~~I/F improvement(HS533/HS667)~~ **Inline encryption(HCI)** CQ improvement(HCI) HS400 tuning

UFS				
Ver.	**1.0/1.1**	**2.0**	**2.1**	**x.x**
Stdndard	**JESD220 / 220A**	**JESD220B**	**tbd**	**tbd**
Publication	**Feb.'11 / Jun.'12 (done)**	**Sep.'13 (done)**	**Mar.'16(tbd)**	**Sep'17(tbd)**
Main New feature on consensus list	Initial ver. HS-G2 Single-lane support M-PHY2.0 / UniPro1.41	HS-G3 support Multi-lane support M-PHY3.0 / UniPro1.6 Power-Up/down sequence etc.	Editorial change Minor change	**UFS Lite** - **Remove LCC feature** - **Remove PWM-G2-4** - **Relax the timing, etc,** **UFS Card**
Main Proposal Under discussion	n/a	n/a	Inline encryption(HCI) Multiple LU(8->32) etc.	HS-G4Bx2 New topology etc.

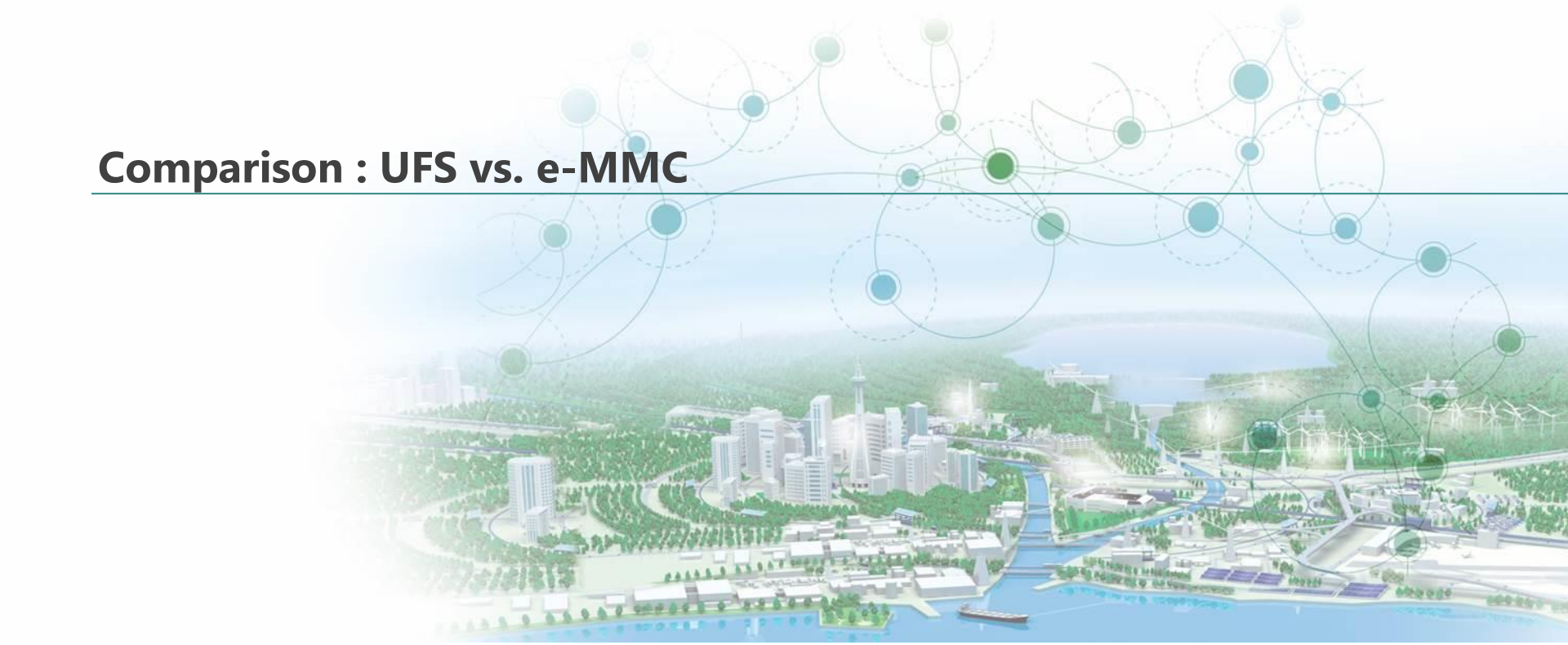
Memory I/F Trend on Mobile Application

❖ Toshiba estimation

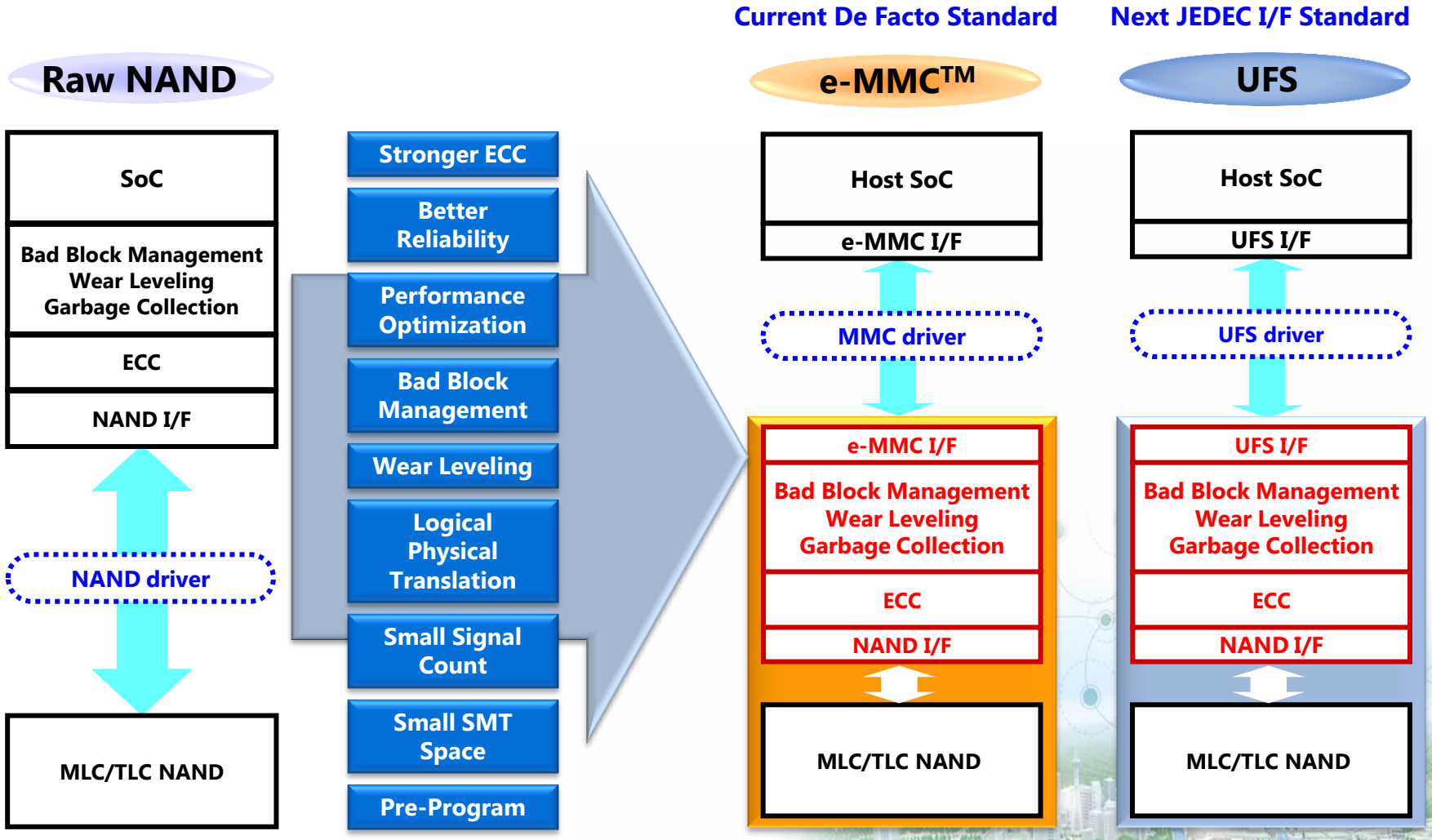
UFS memory will be applied to High-tier smartphone in 2015. After that in Mid/Low-tier area, UFS will replace e-MMC memory step-by-step in 2016 or later.

Application	OS	Memory		2015	2016	2017
High-tier Smartphone 	Android Windows BlackBerry	Storage	I/F	e-MMC V5.1 UFS V2.0	V5.1 V2.0/2.1	V5.x V2.1
			Density	16GB-128GB	32GB-128GB	64GB-256GB
		Removable Card		SD2.0 / 3.0 / 4.0 (UHS)	SD2.0 / 3.0 / 4.0 (UHS)	SD3.0 / 4.0 (UHS)
		DRAM		LPDDR3 / LPDDR4	LPDDR3 / LPDDR4	LPDDR4
Mid-tier Smartphone 	Android Windows BlackBerry	Storage	I/F	e-MMC V5.1 UFS	V5.1 V2.0/2.1	V5.x V2.1
			Density	8GB-32GB	16GB-64GB	32GB-128GB
		Removable Card		SD2.0 / 3.0 / 4.0 (UHS)	SD2.0 / 3.0 / 4.0 (UHS)	SD3.0 / 4.0 (UHS)
		DRAM		LPDDR3 / LPDDR4	LPDDR3 / LPDDR4	LPDDR4
Low-tier smartphone 	Android Windows BlackBerry	Storage	I/F	e-MMC V5.0/5.1 UFS	V5.1	V5.x V2.1
			Density	4-16GB	8-32GB	16GB-64GB
		Removable Card		SD2.0 / 3.0 / 4.0 (UHS)	SD2.0 / 3.0 / 4.0 (UHS)	SD3.0 / 4.0 (UHS)
		DRAM		LPDDR3	LPDDR3	LPDDR3/LPDDR4
2-in-1 PC Tablet 	Android Windows	Storage	I/F	e-MMC V5.1 UFS	V5.1 V2.0/2.1	V5.x V2.1
			Density	16-128GB	32-256GB	64GB-256GB
		Removable Card		SD2.0 / 3.0 / 4.0 (UHS)	SD2.0 / 3.0 / 4.0 (UHS)	SD3.0 / 4.0 (UHS)
		DRAM		LPDDR3 / LPDDR4	LPDDR4 / DDR4?	LPDDR4 / DDR4?

Comparison : UFS vs. e-MMC



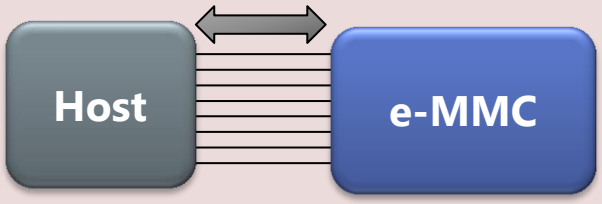
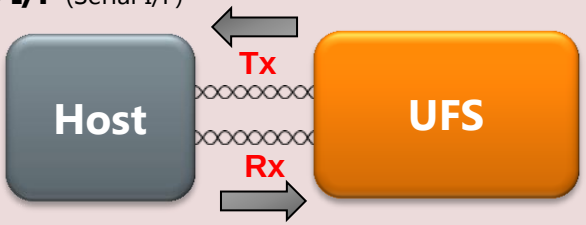
Comparison : UFS vs. e-MMC(1)



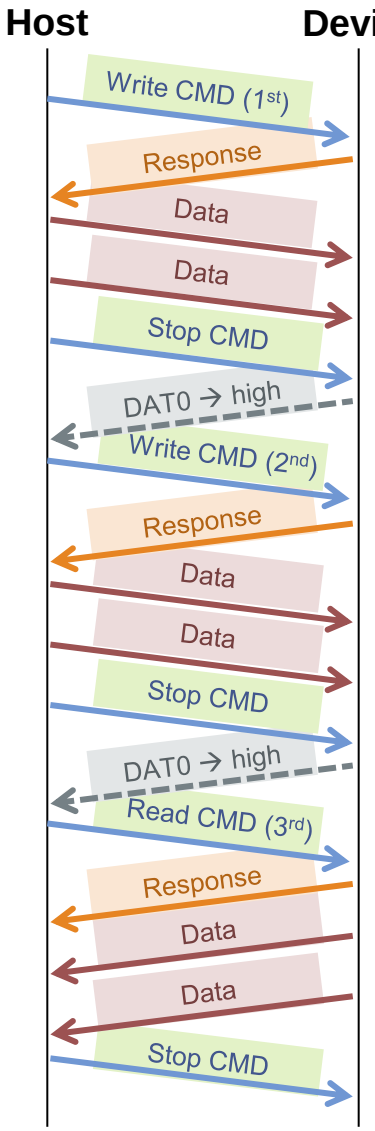
Embedded controller solution can provide better Raw NAND Management.

Comparison : UFS vs. e-MMC(2)

e-MMC features Parallel I/F which has a restriction for further performance improvement beyond HS400(400bps). Meanwhile, UFS features high-speed serial I/F which maintains a performance scalability to extend in the future.

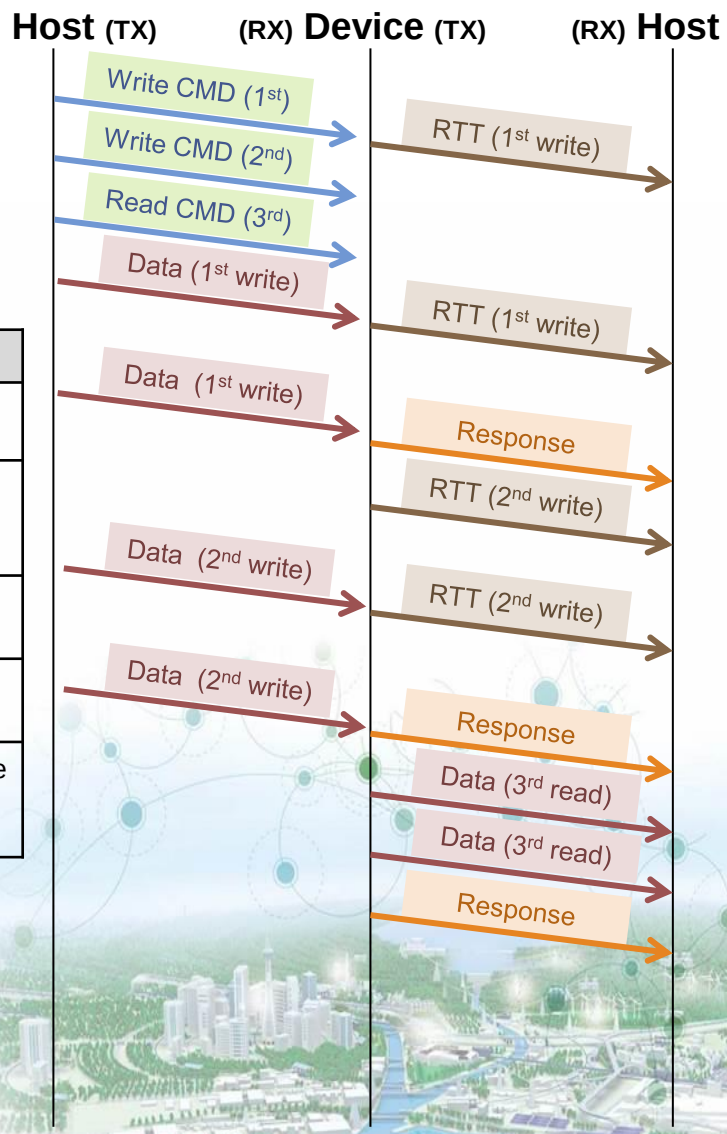
		e-MMC	UFS
Year		Since 2007	Market adoption started in 2015
I/F	Architecture	**MMC I/F** (Bus, Parallel I/F) 	**UFS I/F** (Serial I/F) 
	Speed	**400Mbps** (=400MB/s, Ver.5.0) *Restricted for further improvement	**5.8Gbps** x 2 Lanes (=1160MB/s, Ver.2.0)
	Pin count	**11** (8 I/O and 3 control)	**6** (4 I/O and 2 control) or **10** (in case of 2 lanes)
	Signal amp.	**1.8V** or **1.2V**	**400mVp-p**
	Duplex	**Half** (In serial to send and/or receive the data)	**Full** (Simultaneously to send and receive the data.)
Command Queue		**Supported from Ver.5.1**	**Support**
Command Set		**MMC**	**SCSI**

Comparison : UFS vs. e-MMC(3) Data transfer

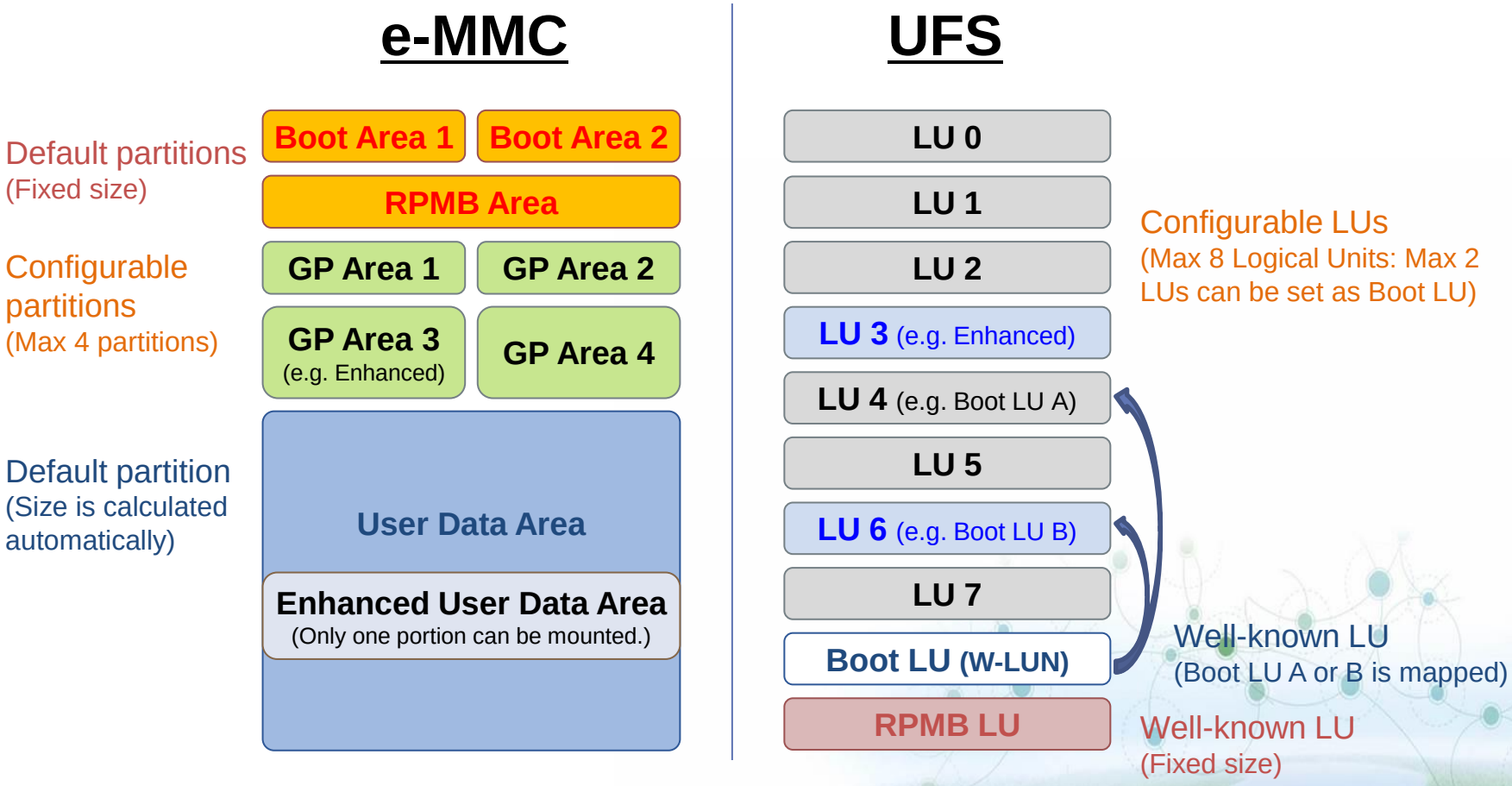


e-MMC ⟵ ⟶ **UFS** (w/ Command Queuing)

	e-MMC	UFS
Queuing	Not available	Available
Response	After Command-Receive	After Command-Execution
Transfer unit [Byte]	512	4KB – 32KB
Timing for Data Transfer	DAT0 line is High	After receive of Ready to Transfer
Notice for finish of Command-Execution	Write: DAT0 line becomes High Read: n/a	Send the response



Comparison : UFS vs. e-MMC(4) LU/Partition

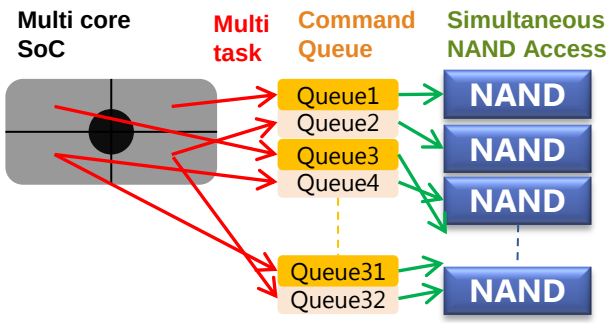


***Each configurable partition and LU can be set as enhanced memory**

Comparison : UFS vs. e-MMC(5) Protocol-1

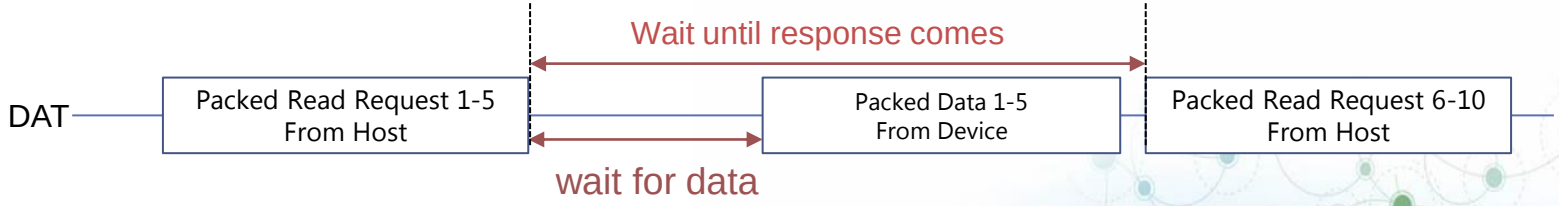
Multi task on UFS memory

UFS can make the difference on Multi Task access from the host.

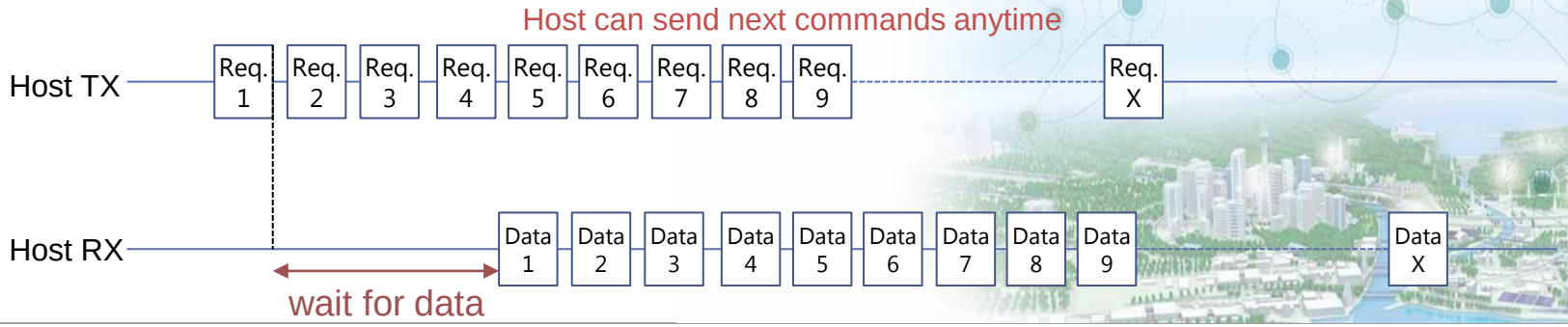


SoC		UFS	e-MMC
Multi Core SoC & Multi Task	Issue multiple command	Multi task will be executed in parallel.	Handled by sequential.
Command(CMD) Queue	Add Task No./ID to each command	Task reorder will be implemented.	There are only simple rule for Task reorder.
Simultaneous NAND Access	Reduce idle time on SoC side	Intelligent memory controller can simultaneously access to each NAND Flash.	Access will sequentially happen to each NAND Flash.

eMMC (Half duplex and Packed CMD)



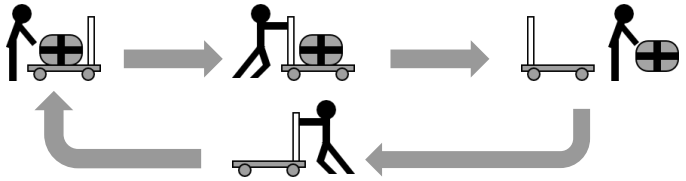
UFS (Full duplex and Command Queuing)



Comparison : UFS vs. e-MMC(6) Protocol-2

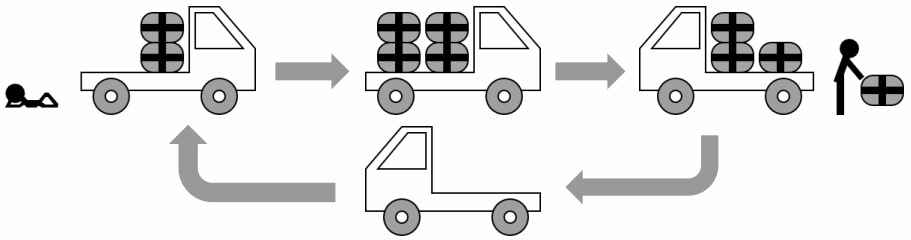
e-MMC (Legacy) : Push-car type

- Luggage have to be carried one by one.
- 2nd luggage cannot be carried until push car comes back.



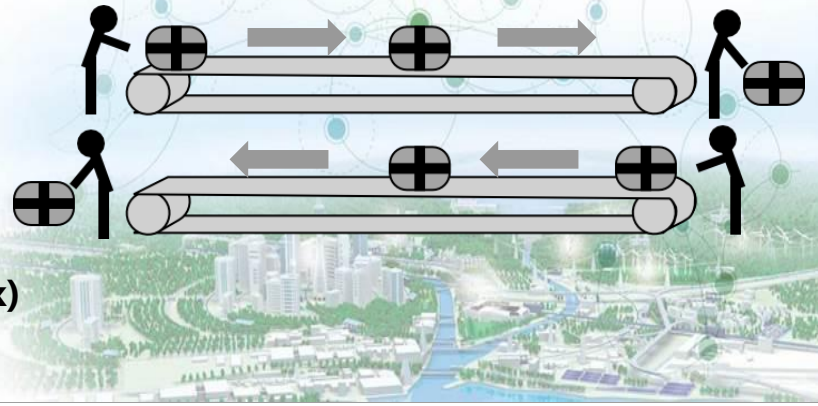
e-MMC (Packed Command) : Truck type

- Many luggage can be delivered at once.
- Efficiency is not so good.
- Only same kind of luggage can be delivered.
- 2nd batch cannot be carried until truck returns.



UFS (Command Queuing) : Belt-conveyor type

- Many luggage can be delivered at once.
- Operator just can put on the belt.
- There are 2 belts (i.e. Receiver and Transfer lane)
  (Only 1 belt can be used in the case of e-MMC.)
- Many operators can simultaneously work (i.e. Multi Task)



Package signal assignment (Top view)

2nd lane

Toshiba UFS will NOT use these pins.

Reserved for Chain Topology

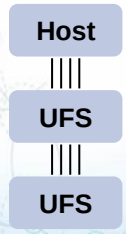
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	VDDiQ	VCCQ	VCCQ	VCCQ2	VCCQ2	VDDiQ2	VDDi	CPOUT1	C-	C+	NC	NC
B	NC	VSS	RFU	VCCQ	VCCQ	VCCQ2	VCCQ2	VCC	VCC	CPOUT2	VSS	VSS	RFU	NC
C	VSS	VSS	VSS	VCCQ	VCCQ	VCCQ2	VCCQ2	VCC	VCC	RFU	VSS	VSS	RFU	RFU
D	DIN1_t	DIN1_c	VSS	Index								VSS	VSS	VSS
E	VSS	VSS	VSS		VCCQ	VSF1	VSF2	VCC	VSF3	VSF4		VSS	RFU	RFU
F	DIN0_t	DIN0_c	VSS		VCCQ					VSF5		VSS	VSS	VSS
G	VSS	VSS	VSS		VSF6					VSS		VSS	RFU	RFU
H	REF_CLK	RST_n	VSS		VSS					VSS		VSS	VSS	VSS
J	VSS	VSS	VSS		VSS					VSF7		VSS	RFU	RFU
K	DOUT0_c	DOUT0_t	VSS		VSS	VCCQ2	VCCQ2	VCC	NC	VSF8		VSS	VSS	VSS
L	VSS	VSS	VSS									VSS	RFU	RFU
M	DOUT1_c	DOUT1_t	VSS	VSS	VSS	RFU	RFU	NC	NC	RFU	NC	VSS	VSS	VSS
N	NC	VSS	VSS	VSS	VSS	RFU	RFU	VCC	VCC	RFU	VSS	VSS	RFU	NC
P	NC	NC	RFU	VSS	VSS	RFU	RFU	VCC	VCC	VSF9	VSS	VSS	NC	NC

UFS2.0

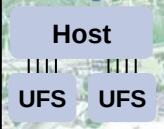
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	DAT0	DAT1	DAT2	RFU	RFU	NC	NC	NC	NC	NC	NC	NC
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC
C	NC	VDDi	NC	VssQ	NC	VccQ	NC	NC	NC	NC	NC	NC	NC	NC
D	NC	NC	NC	Index								NC	NC	NC
E	NC	NC	NC		RFU	VCC	VSS	RFU	VSF1	VSF2		NC	NC	NC
F	NC	NC	NC		VCC					VSF3		NC	NC	NC
G	NC	NC	RFU		VSS					RFU		NC	NC	NC
H	NC	NC	NC		VSF4					VSS		NC	NC	NC
J	NC	NC	NC		VSF5					VCC		NC	NC	NC
K	NC	NC	NC		RST_n	VSF6	VSF7	VSS	VCC	VSF8		NC	NC	NC
L	NC	NC	NC									NC	NC	NC
M	NC	NC	NC	VccQ	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC
N	NC	VssQ	NC	VccQ	VssQ	NC	NC	NC	NC	NC	NC	NC	NC	NC
P	NC	NC	VccQ	VssQ	VccQ	VssQ	RFU	NC	NC	VSF9	NC	NC	NC	NC

e-MMC

Chain Topology Image



Point to Point Image



Toshiba Gen.3 UFS2.0 pin out & debugging pin

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	VDDiQ	VCCQ	VCCQ	VCCQ2	VCCQ2	VDDiQ2	VDDi	CPOUT1	C-	C+	NC	NC
B	NC	VSS	RFU	VCCQ	VCCQ	VCCQ2	VCCQ2	VCC	VCC	CPOUT2	VSS	VSS	RFU	NC
C	VSS	VSS	VSS	VCCQ	VCCQ	VCCQ2	VCCQ2	VCC	VCC	RFU	VSS	VSS	RFU	RFU
D	DIN1 _t	DIN1 _c	VSS	Index								VSS	VSS	VSS
E	VSS	VSS	VSS		VCCQ	VSF1	VSF2	VCC	VSF3	VSF4		VSS	RFU	RFU
F	DIN0 _t	DIN0 _c	VSS		VCCQ					VSF5		VSS	VSS	VSS
G	VSS	VSS	VSS		VSF6					VSS		VSS	RFU	RFU
H	REF _CLK	RST _n	VSS		VSS					VSS		VSS	VSS	VSS
J	VSS	VSS	VSS		VSS					VSF7		VSS	RFU	RFU
K	DOUT0 _c	DOUT0 _t	VSS		VSS	VCCQ2	VCCQ2	VCC	NC	VSF8		VSS	VSS	VSS
L	VSS	VSS	VSS									VSS	RFU	RFU
M	DOUT1 _c	DOUT1 _t	VSS	VSS	VSS	RFU	RFU	NC	NC	RFU	NC	VSS	VSS	VSS
N	NC	VSS	VSS	VSS	VSS	RFU	RFU	VCC	VCC	RFU	VSS	VSS	RFU	NC
P	NC	NC	RFU	VSS	VSS	RFU	RFU	VCC	VCC	VSF9	VSS	VSS	NC	NC

Debug Signal pin 8pin

Top View

Toshiba Gen.4 UFS2.0 pin out & debugging pin

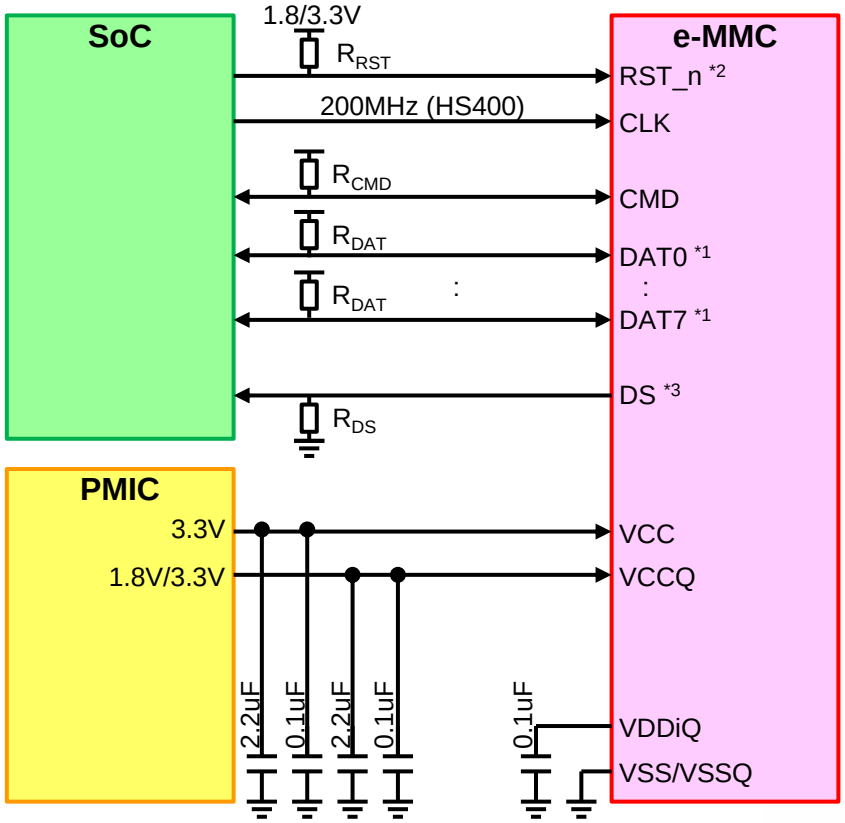
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	VDDiQ	VCCQ	VCCQ	VCCQ2	VCCQ2	VDDiQ2	VDDi	CPOUT1	C-	C+	NC	NC
B	NC	VSS	RFU	VCCQ	VCCQ	VCCQ2	VCCQ2	VCC	VCC	CPOUT2	VSS	VSS	RFU	NC
C	VSS	VSS	VSS	VCCQ	VCCQ	VCCQ2	VCCQ2	VCC	VCC	RFU	VSS	VSS	RFU	RFU
D	DIN1 _t	DIN1 _c	VSS	Index								VSS	VSS	VSS
E	VSS	VSS	VSS		VCCQ	VSF1	VSF2	VCC	VSF3	VSF4		VSS	RFU	RFU
F	DIN0 _t	DIN0 _c	VSS		VCCQ					VSF5		VSS	VSS	VSS
G	VSS	VSS	VSS		VSF6					VSS		VSS	RFU	RFU
H	REF _CLK	RST _n	VSS		VSS					VSS		VSS	VSS	VSS
J	VSS	VSS	VSS		VSS					VSF7		VSS	RFU	RFU
K	DOUT0 _c	DOUT0 _t	VSS		VSS	VCCQ2	VCCQ2	VCC	NC	VSF8		VSS	VSS	VSS
L	VSS	VSS	VSS									VSS	RFU	RFU
M	DOUT1 _c	DOUT1 _t	VSS	VSS	VSS	RFU	RFU	NC	NC	RFU	NC	VSS	VSS	VSS
N	NC	VSS	VSS	VSS	VSS	RFU	RFU	VCC	VCC	RFU	VSS	VSS	RFU	NC
P	NC	NC	RFU	VSS	VSS	RFU	RFU	VCC	VCC	VSF9	VSS	VSS	NC	NC

Debug Signal pin
2pin

Top View

Recommended System Design

e-MMC

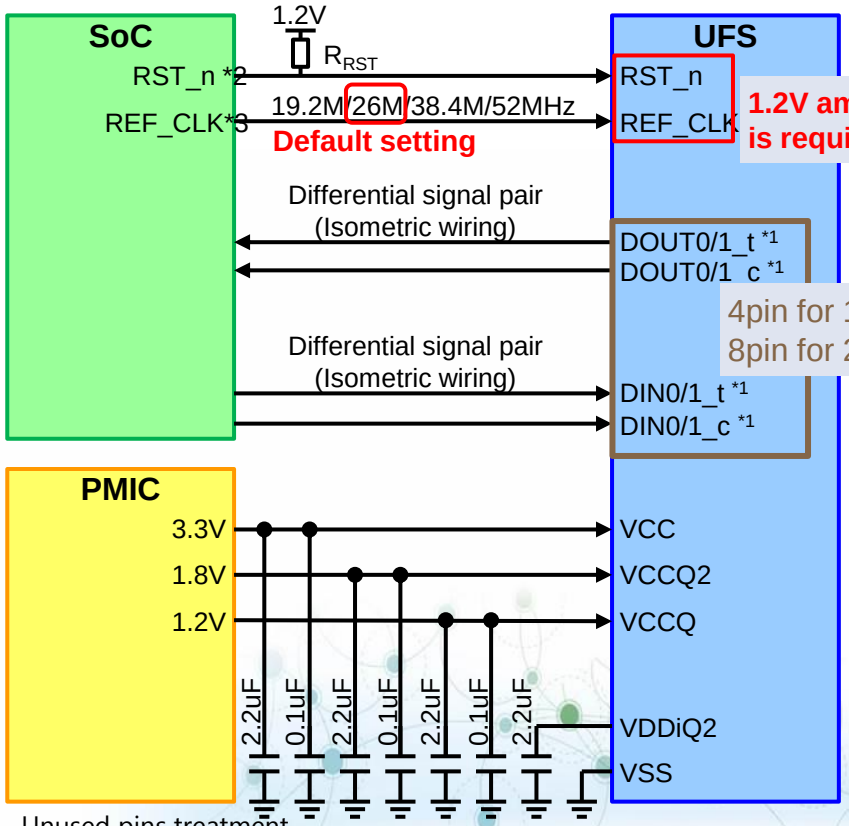


Unused pins treatment

NC	NC or GND	RFU	NC

*1: Please refer to JESD84-B50, Table 179 - Capacitance, about recommended values of resistances.
*2: RST_n might be NC or connected to GND when it is not used. DAT4 - DAT7 should be NC in 4 bit mode.
*3: DS should be left floating in case of not using HS400.

UFS



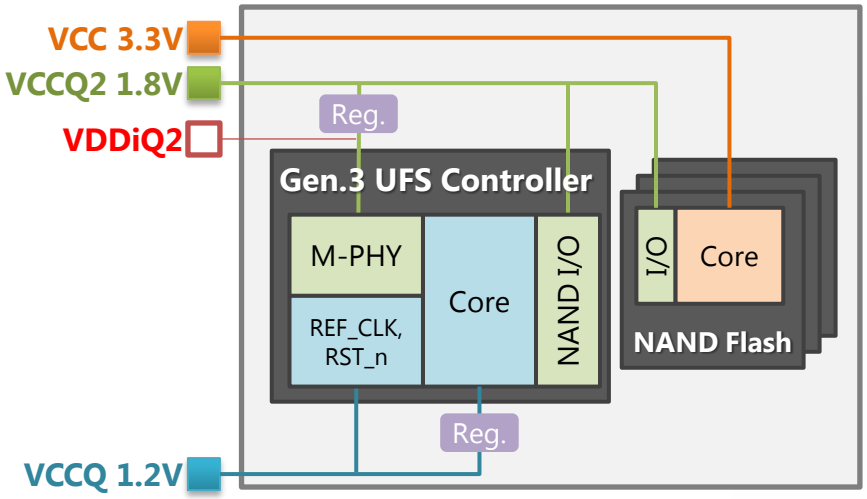
Unused pins treatment

VDDi	NC	VSFn/RFU	NC(=Floating)
VDDiQ	NC	C+/C-	NC or GND
NC	NC or GND	CPOUT1/2	NC or GND

*1: If some of DINn_t/c or DOUTn_t/c are not used, the DINn_t/c is recommended to be connected to GND and DOUTn_t/c is recommended to be left floating.
*2 : Optional feature. Some host would like not to use it because Power-on write protection will be released with this.
*3 : Mandate feature. REF_CLK shall always be required when the device is in HS-mode.

Block diagram : Toshiba 15nm UFS

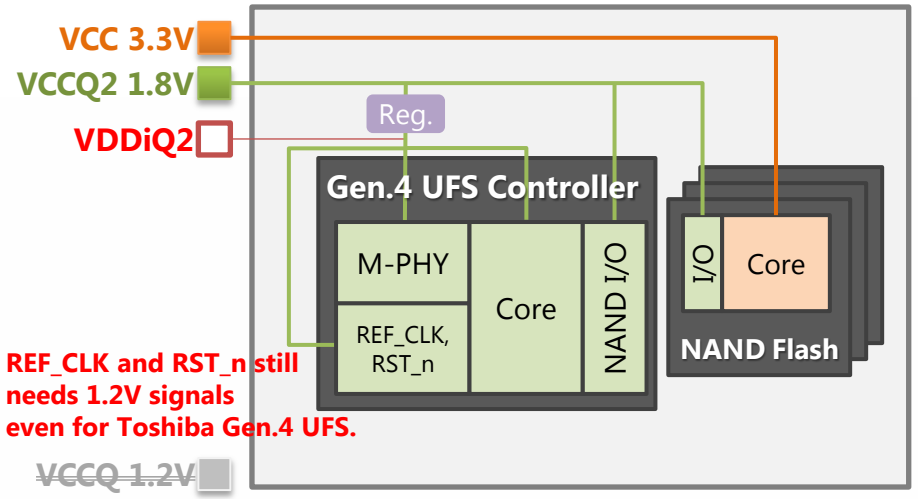
Toshiba "Gen.3" UFS Ver.2.0, 3 power rail



Pin name	VDDiQ2
Apply to	M-PHY
Typical	2.2uF
min.	0.7uF
max.	2.4uF

PMIC for	Required Max. current
VCC (3.3V)	750mA
VCCQ2 (1.8V)	450mA
VCCQ (1.2V)	450mA

Toshiba "Gen.4" UFS Ver.2.0, 2 power rail

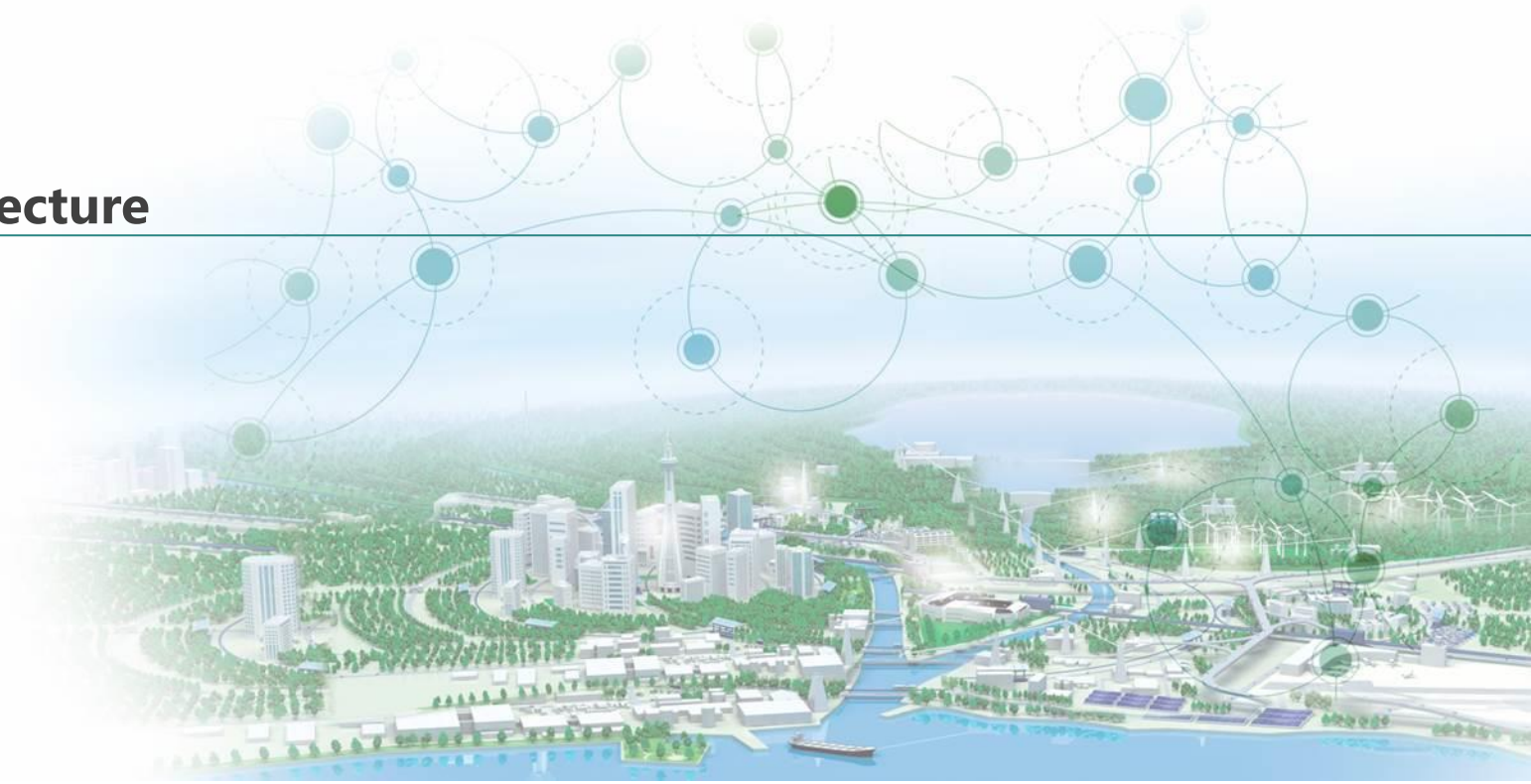


Pin name	VDDiQ2
Apply to	M-PHY
Typical	2.2uF
min.	0.7uF
max.	2.4uF

PMIC for	Required Max. current
VCC (3.3V)	600mA
VCCQ2 (1.8V)	700mA
VCCQ (1.2V)	N/A

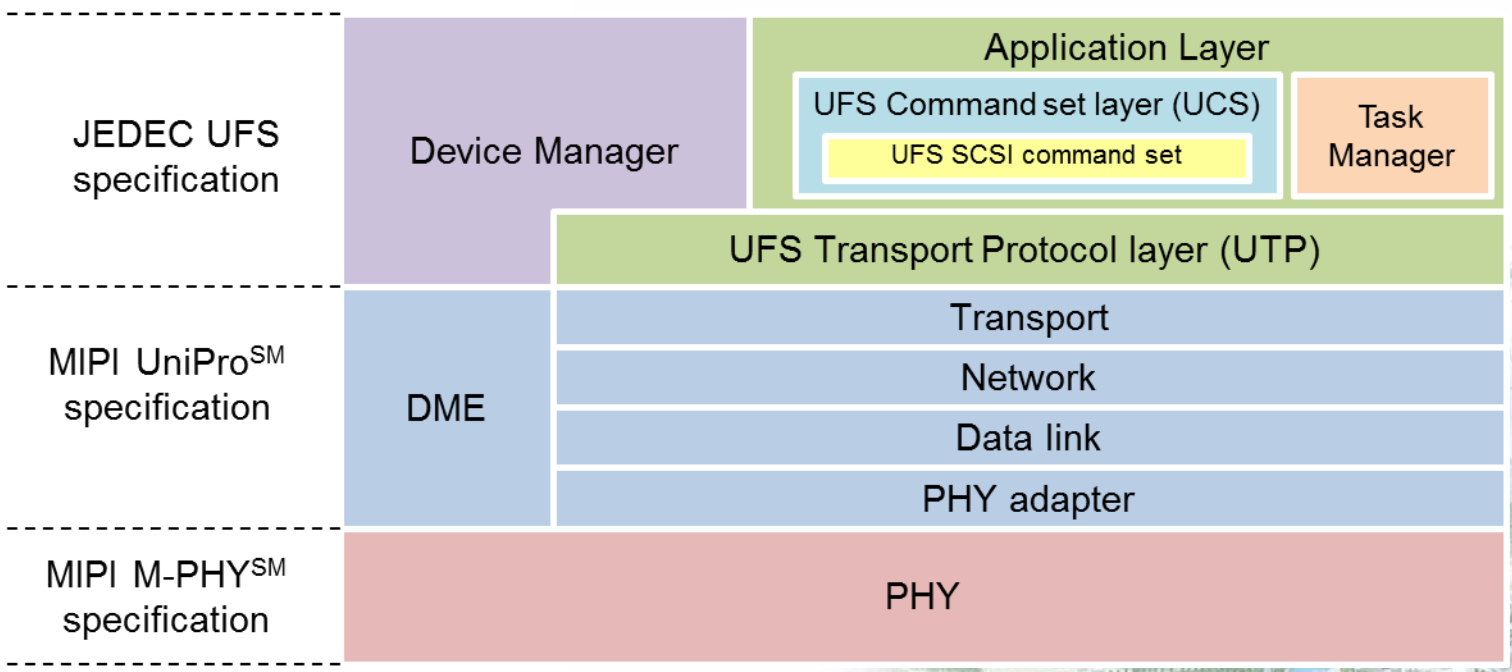
Please prepare the suitable VDDiQ2(Cap.) and LDO (PMIC) accordingly

UFS architecture



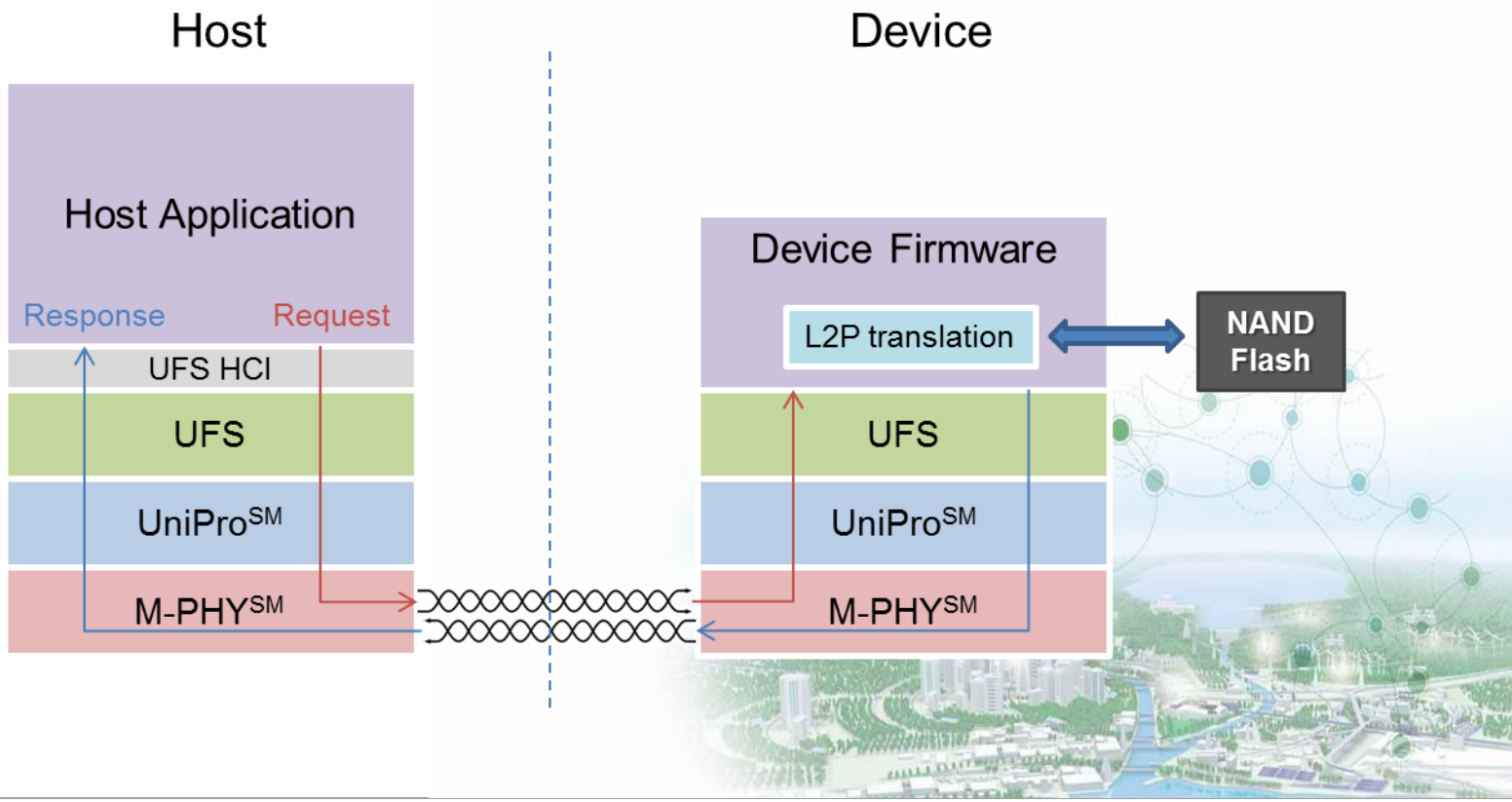
UFS protocol layer structure

- **UFS adopts protocol stack architecture like OSI reference model**
  - Layer 1: M-PHY[SM], which is defined by MIPI
  - Layer 1.5-4: UniPro[SM], which is defined by MIPI
  - Layer 5-7: UFS, which is defined by JEDEC
- **UFS specification defines 3 command types**
  - Basic command (SCSI only in v2.0): Handled by UCS (Read/Write, etc.)
  - Task Management Request: Handled by Task Manager (abort/cancel task, etc.)
  - Query Request: Handled by Device Manager (access to descriptor, etc.)

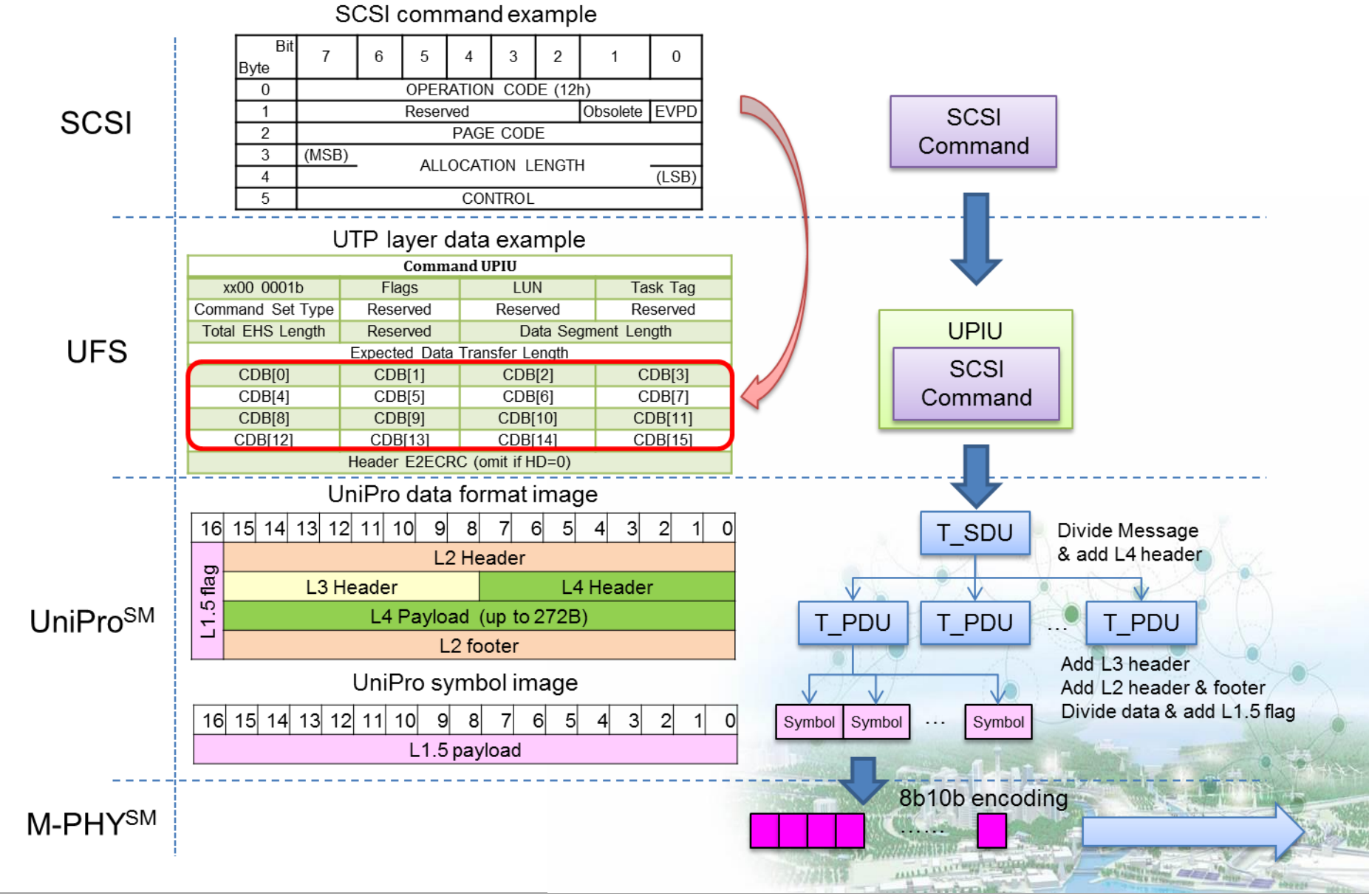


Host/Device Connection image

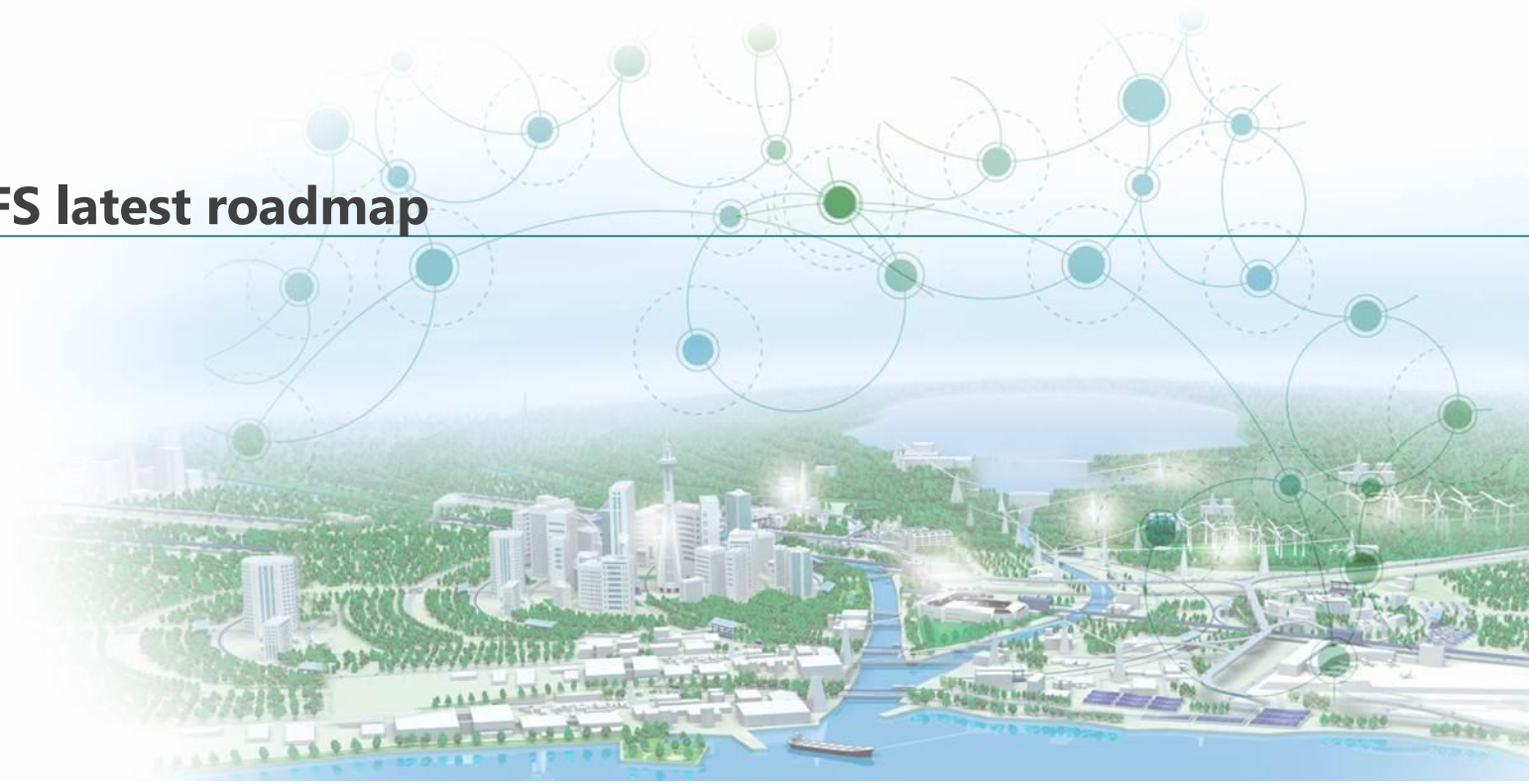
- **Both host and device have same protocol stack under UFS layer**
- **Host application accesses to device through UFS Host Controller Interface (UFS HCI)**
  - UFS HCI is also standardized by JEDEC



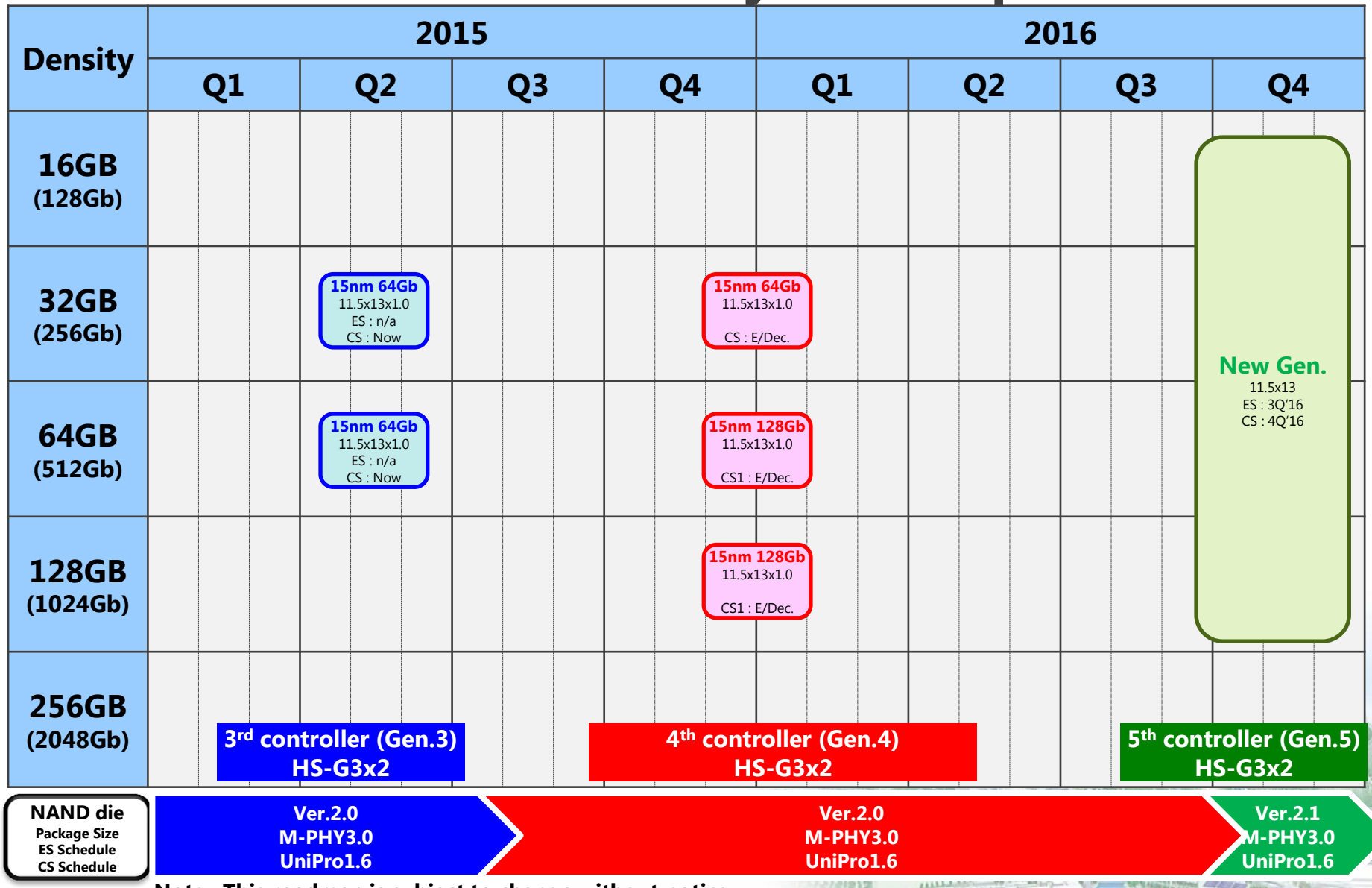
UFS data flow image in host controller



Toshiba UFS latest roadmap



Toshiba UFS Ver.2.0 memory roadmap



Note : This roadmap is subject to change without notice and does not include EOL schedule.

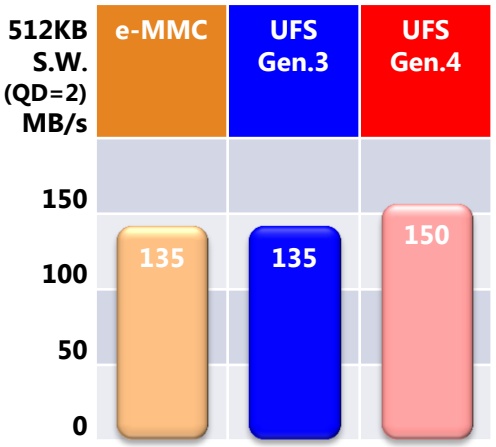
Toshiba UFS Performance data

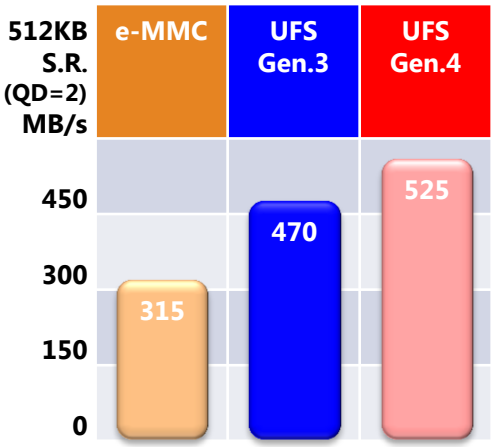
This data is subject to change without notice.

UFS Ver.						Ver.2.0				Ver.2.0(2.1)					
Power mode						HS-G3B									
Controller Generation						Gen.3				Gen.4					
NAND Chip						15nm 64Gb				15nm 64Gb		15nm 128Gb			
Density & Interleave						32GB (4-Int.)		64GB (8-Int.)		32GB (4-Int.)		64GB (4-Int.)		128GB (4-Int.)	
Package (BGA)						11.5x13x1.0		11.5x13x1.2		11.5x13x1.0					
CS schedule						Now		Now		12/E		12/E		11/E(CS0)	
# of lane						1	2	1	2	1	2	1	2	1	2
Performance	Sequential [MB/s]	QD:2 (FUA=0)	512KB chunk	Read		470	520	470	520	525	610	525	610	525	610
				Write	Normal	135	135	165	170	153	153	153	153	153	153
					Enhanced	180	180	180	180	285	285	285	285	285	285
			256KB chunk	Read		440	480	440	480	520	610	520	610	520	610
				Write	Normal	90	100	110	120	150	150	150	150	150	150
					Enhanced	150	160	150	160	285	285	285	285	285	285
	Random [IOps]	QD:8	4KB chunk	Read		23K	23K	30K	30K	25K	25K	25K	25K	25K	25K
				Write	Cache-on	7.0K	7.0K	7.2K	7.2K	15K	15K	15K	15K	15K	15K
					Cache-off	4.0K	4.0K	4.0K	4.0K	2.3K	2.3K	2.3K	2.3K	2.3K	2.3K
Average Current/Power VCC = 3.3V VCCQ = 1.2V VCCQ2= 1.8V Ta = RT	Read	400MB chunk		IccQ	[mA]	165	180	155	170	-	-	-	-	-	-
				IccQ2	[mA]	130	175	150	200	325	380	325	380	335	395
				Icc	[mA]	75	80	75	85	70	80	70	80	70	80
				Power	**[mW]**	**680**	**800**	**710**	**850**	**820**	**950**	**820**	**950**	**840**	**980**
	Write	400MB chunk		IccQ	[mA]	130	135	135	140	-	-	-	-	-	-
				IccQ2	[mA]	60	95	75	110	220	280	220	280	230	300
				Icc	[mA]	100	100	155	155	105	105	120	120	120	120
				Power	**[mW]**	**600**	**670**	**810**	**880**	**750**	**860**	**800**	**900**	**810**	**940**
Idle Current / Power (Typical), Recovery=2ms VCC = 3.3V, VCCQ = 1.2V VCCQ2=1.8V, Ta = RT				IccQ	[uA]	420		420		-		-		-	
				IccQ2	[uA]	40		50		240		245		265	
				Icc	[uA]	80		160		85		85		165	
				Power	**[mW]**	**0.84**		**1.12**		**0.71**		**0.72**		**1.02**	
Sleep Current / Power (Typical), Recovery=20ms VCC = 0V, VCCQ = 1.2V VCCQ2=1.8V, Ta = RT				IccQ	[uA]	420		420		-		-		-	
				IccQ2	[uA]	30		35		230		230		240	
				Icc	[uA]	0		0		0		0		0	
				Power	**[mW]**	**0.56**		**0.57**		**0.41**		**0.41**		**0.43**	
						5us window				5us window					
Peak Current (Typical) VCC = 3.6V, VCCQ = 1.3V VCCQ2 = 1.95V, Ta = RT				IccQ	[mA]	305	320	295	310	-	-	-	-	-	-
				IccQ2	[mA]	180	215	205	240	400	450	400	450	400	450
				Icc	[mA]	315	325	465	465	350	360	400	400	480	500
						5us window				5us window					
PeakCurrent Worst (Worst) VCC = 3.6V, VCCQ = 1.3V VCCQ2= 1.95V, Ta = HT				IccQ	[mA]	405	420	400	410	-	-	-	-	-	-
				IccQ2	[mA]	190	225	215	250	600	650	600	650	600	650
				Icc	[mA]	370	373	530	550	450	460	500	500	560	570

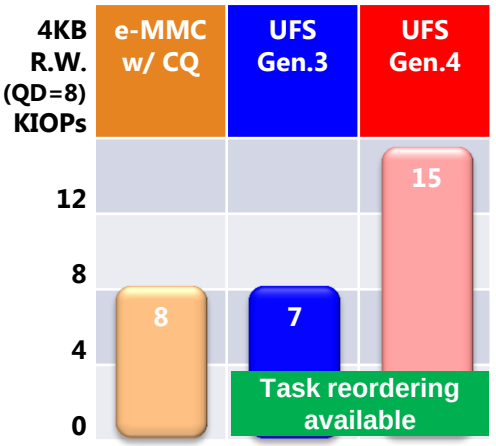
32GB e-MMC/UFS Performance/Power (incl. Target value)

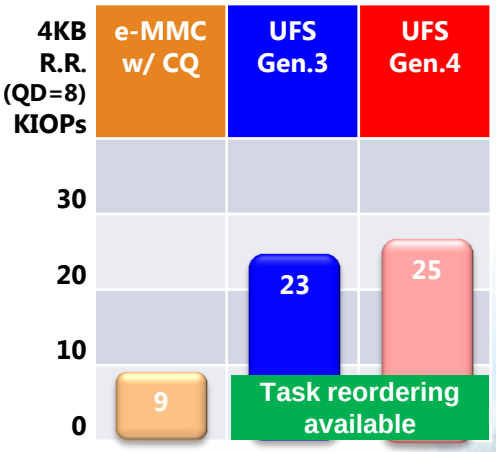
Sequential performance



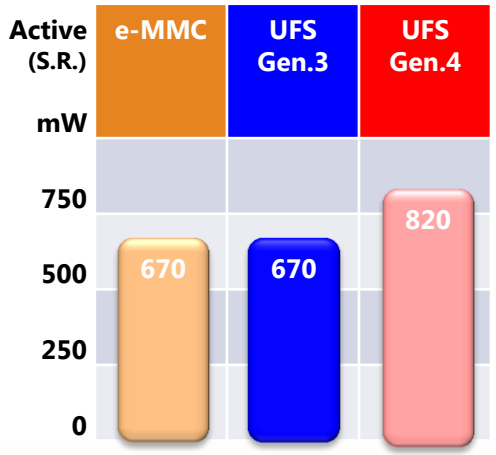


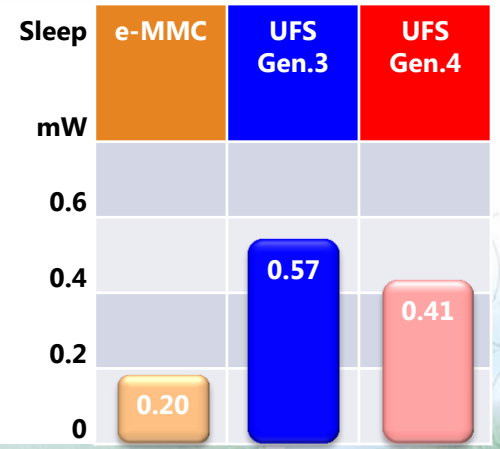
Random performance





Power consumption

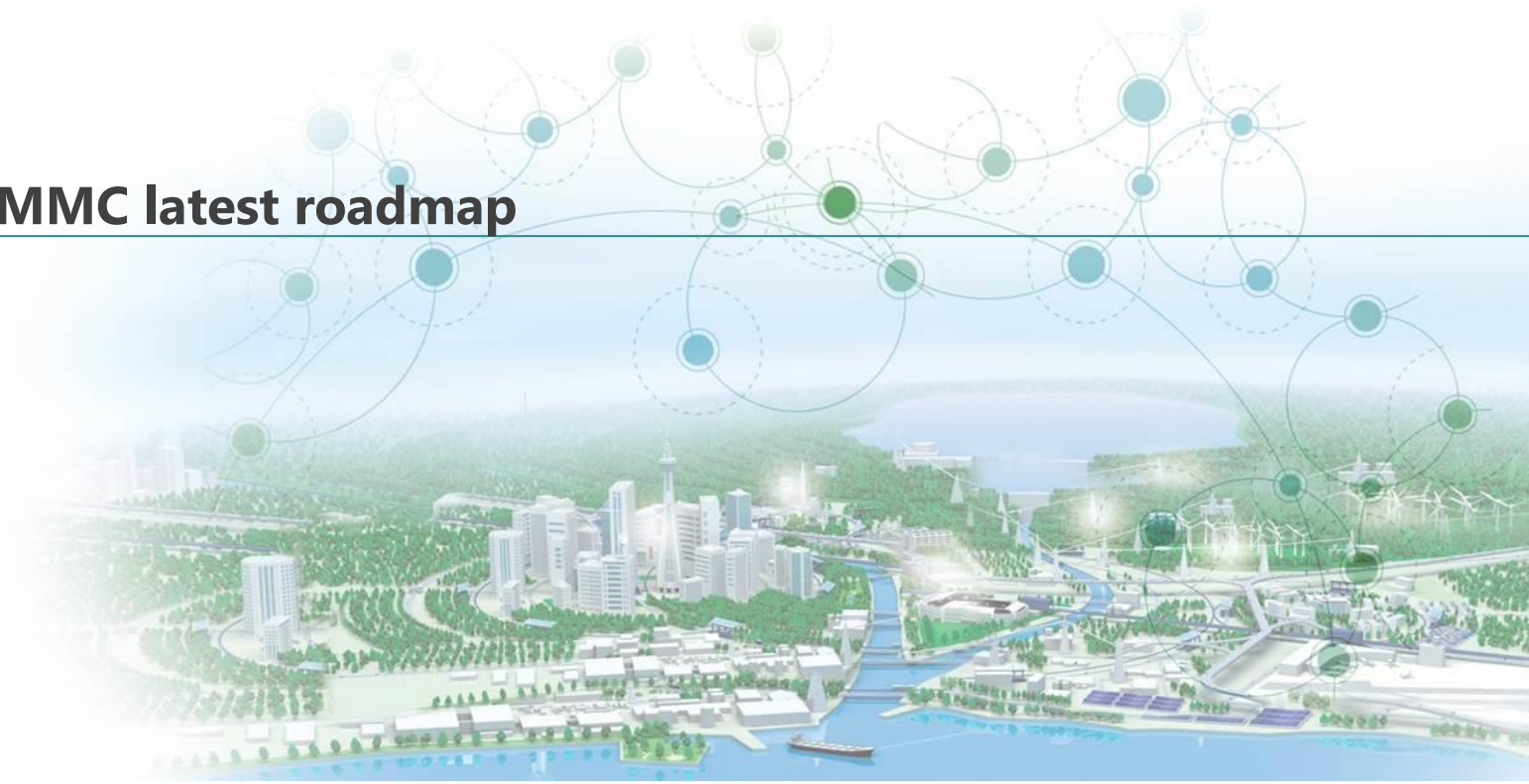




e-MMC Ver.5.1 : HS400 mode
UFS Ver.2.0 : HS-G3Bx1lane

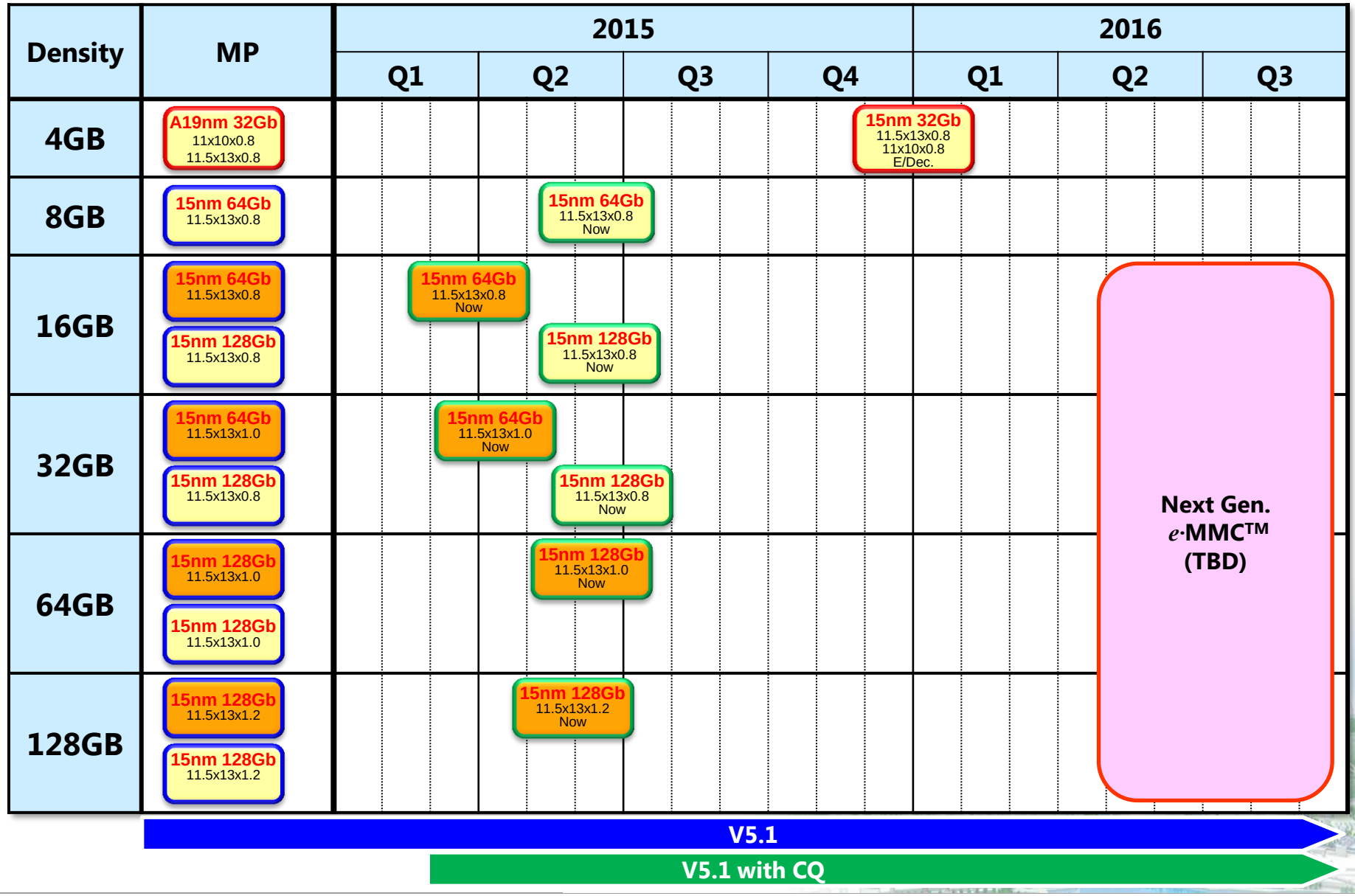
This information is subject to change w/o notice.

Toshiba e-MMC latest roadmap



e·MMC™ Roadmap

e·MMC™ Supreme | e·MMC™ Premium | NAND Gen. Package Size CS Schedule | Seq.W [MB/s]



Supreme+ : Exclusively for 15nm 64GB (64Gb) device only
4GB : V5.0 devices
Note : This roadmap is subject to change without notice.

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