eStorage Market & UFS Seminar

Oct, 2015 l Samsung Memory NAND Marketing

SAMSUNG

NAND Application Trend

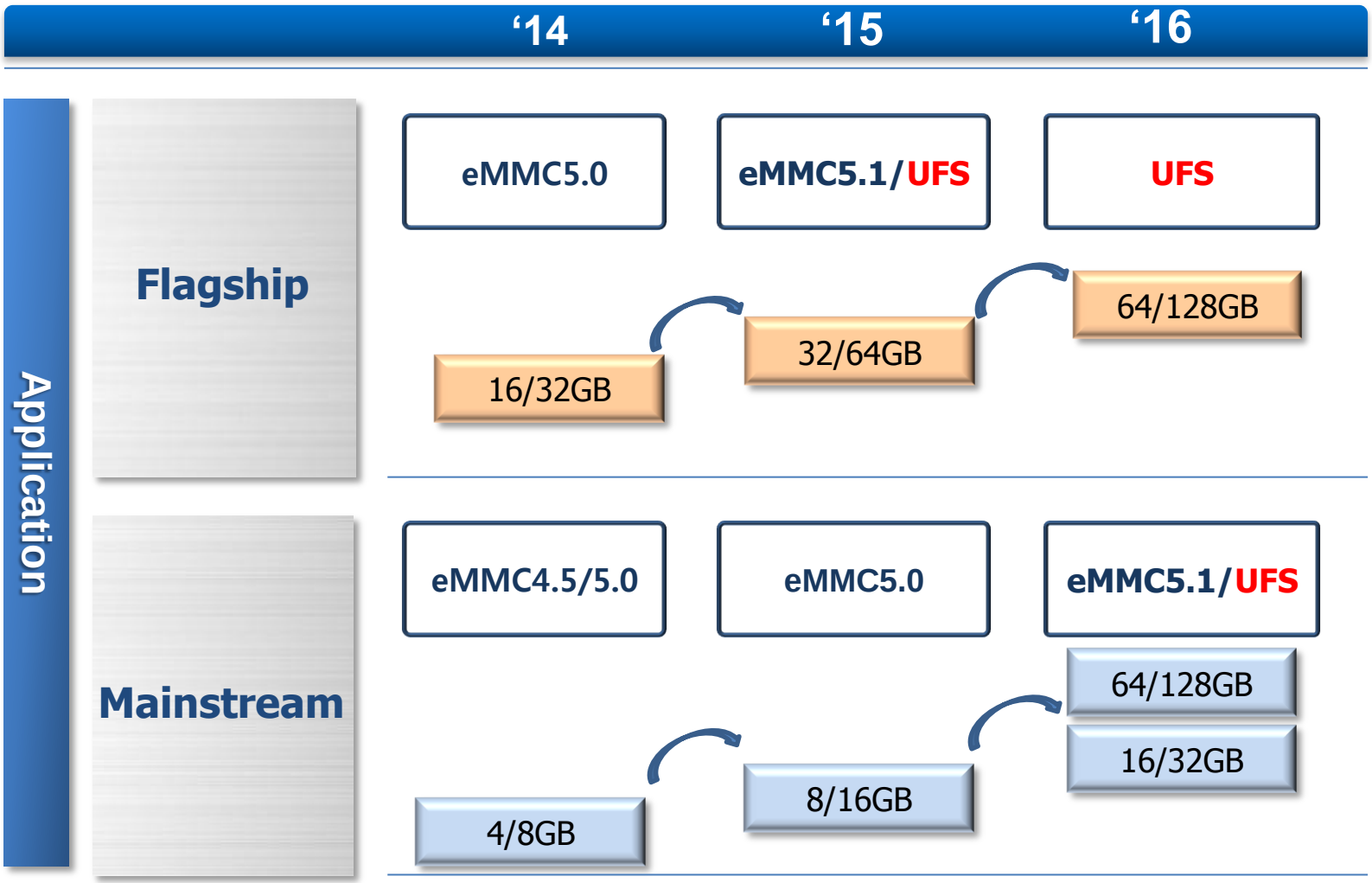
Mobile eStorage and SSD lead NAND market

- More Smartphone demand expected, while less Tablet demand (weaker demand in 7")

	Smart phone	Tablet	SSD
GB/Sys	12.3 → 14.3 (+34%) → 19.0	19.9 → 20.5 (+14%) → 23.5	188.5 → 247.7 (+25%) → 309.2
M Set	1012 → 1,210 (+16%) → 1,401 (Prev. 1,390M)	223 → 240 (-2%) → 234 (Prev. 238M)	50 → 61 (+32%) → 80
	2013 → 2014 → 2015	2013 → 2014 → 2015	2013 → 2014 → 2015
NAND TAM (BGB)	12.5 → 17.3 (+55%) → 26.7	4.4 → 4.9 (+12%) → 5.5	9.4 → 15.0 (+65%) → 24.7
Solutions	eMMC, eMCP, MCP → eMMC/UFS, eMCP, MCP	eMMC, eMCP, Comp → eMMC, eMCP, Comp	SATA, SAS → SATA, SAS, PCIe

Mobile Market Segmentation by eStorage

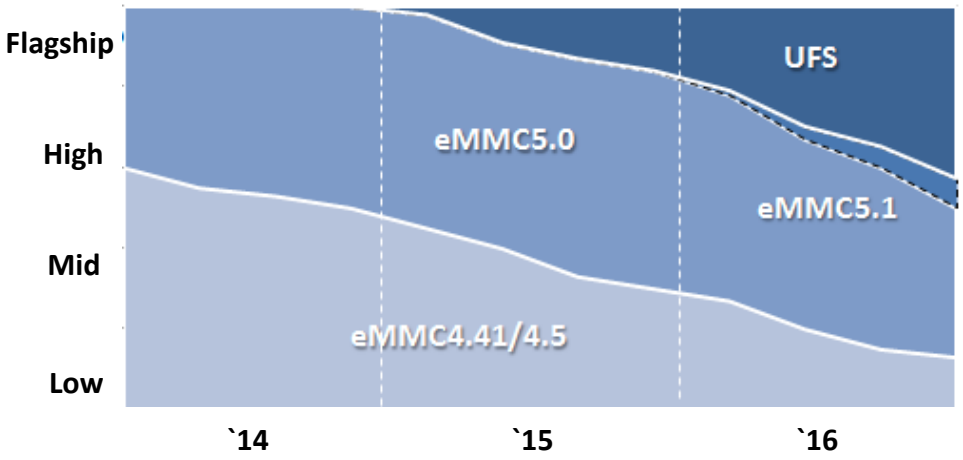
- Differentiation in flagship with 64/128GB UFS
- Steady U/X in mainstream with 16~128GB eMMC 5.1



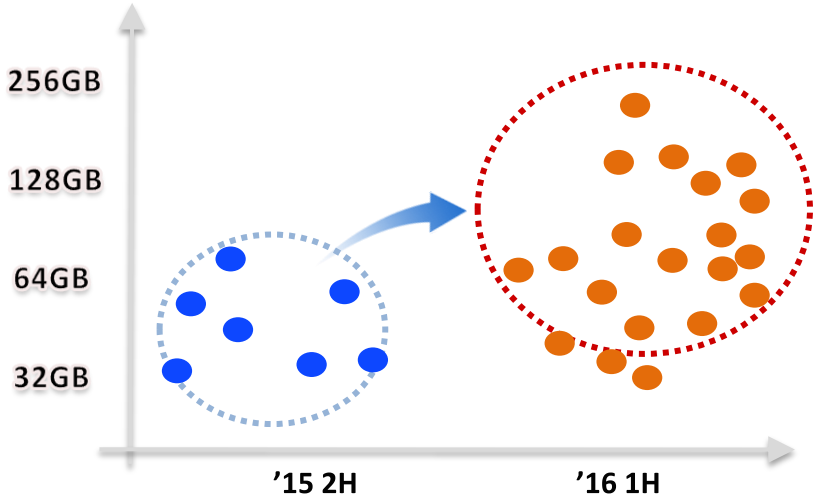
Projection of UFS Penetration

- **UFS adoption in High-end**
- **Mid-range penetration is expected to start in ’16. 3Q**
  - 1 Year lagging adoption behind high-end

Mobile solution 채용 예상

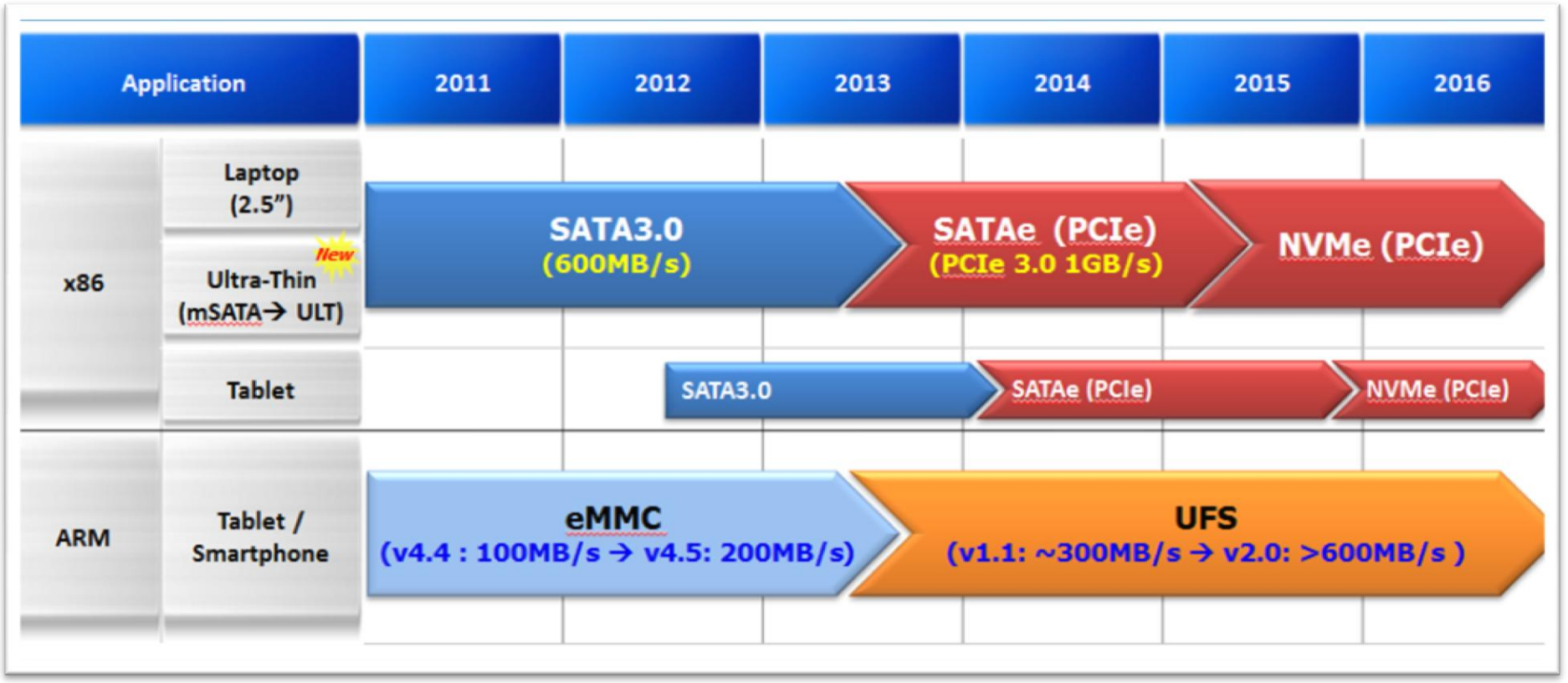


업체별 UFS 채용 예상



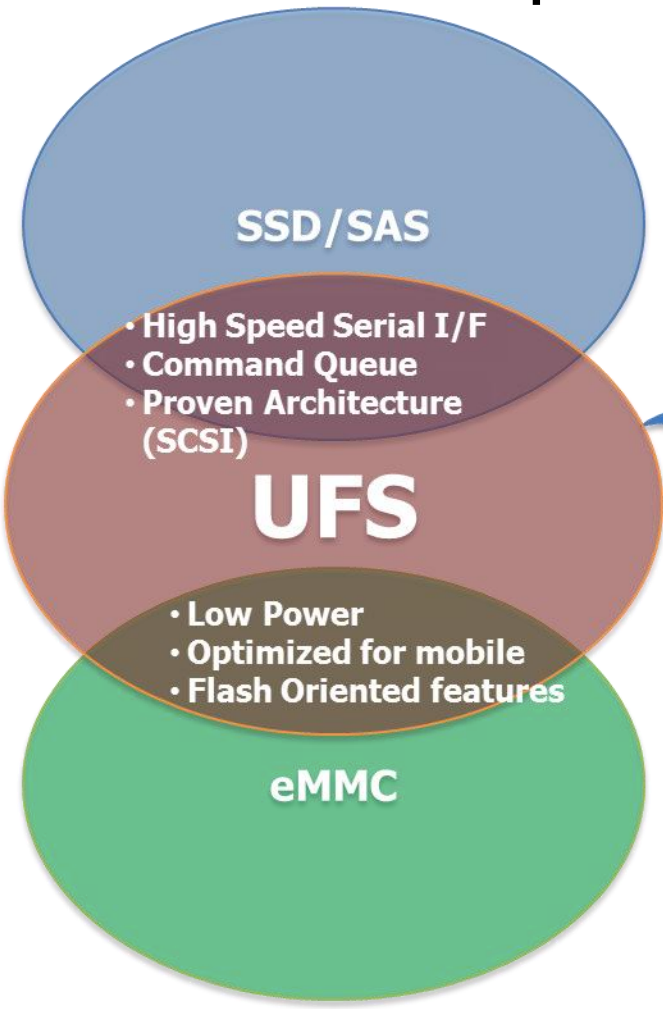
Flash Memory Interface 변화 Trend

- **Higher speed Interface로의 변화**
  - eStorag: eMMC(Max 400Mbps) → UFS(Max 6Gbps)



UFS Concept

Small SSD in Smartphone

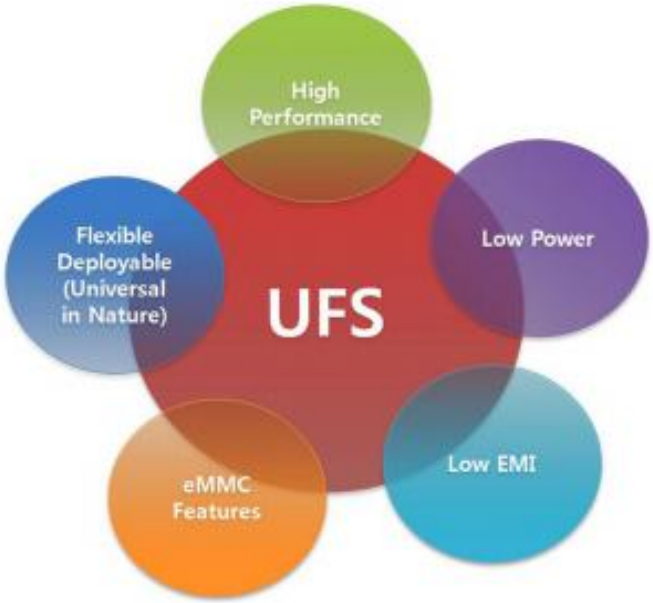


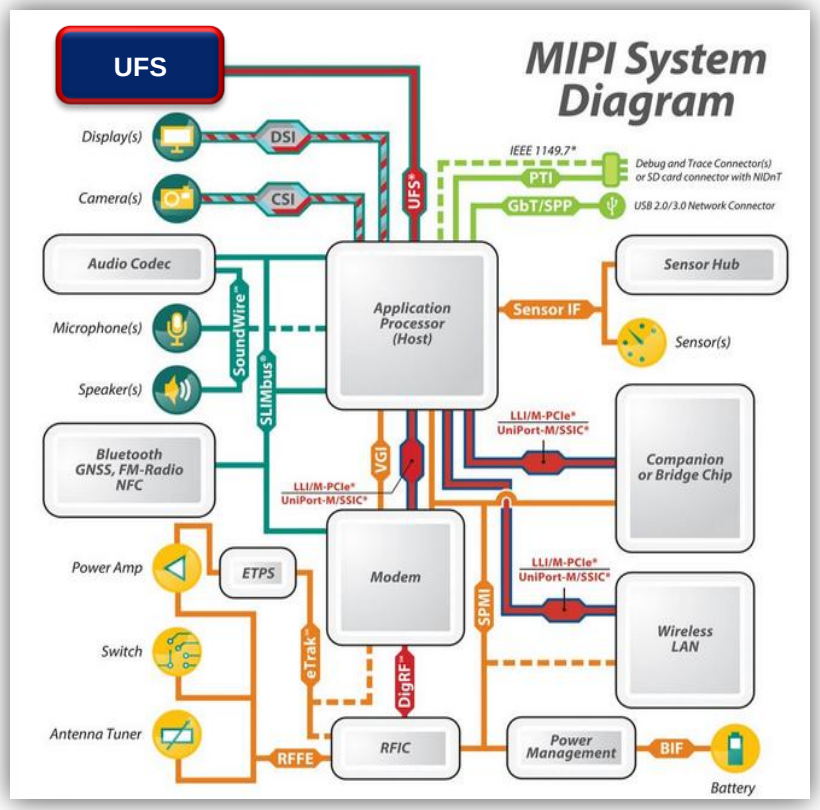
SSD in Smartphone

- Better User Experience
- Fast Boot
- Fast Response
- Fast File Copy

UFS 장점

- High Speed Host Interface[<6Gbps/lane]
- Low EMI
- Dual Simplex channel enables “Read While Write” or opposite ops.
- Command Queuing- Device has capability to server up to 32 command at the same time

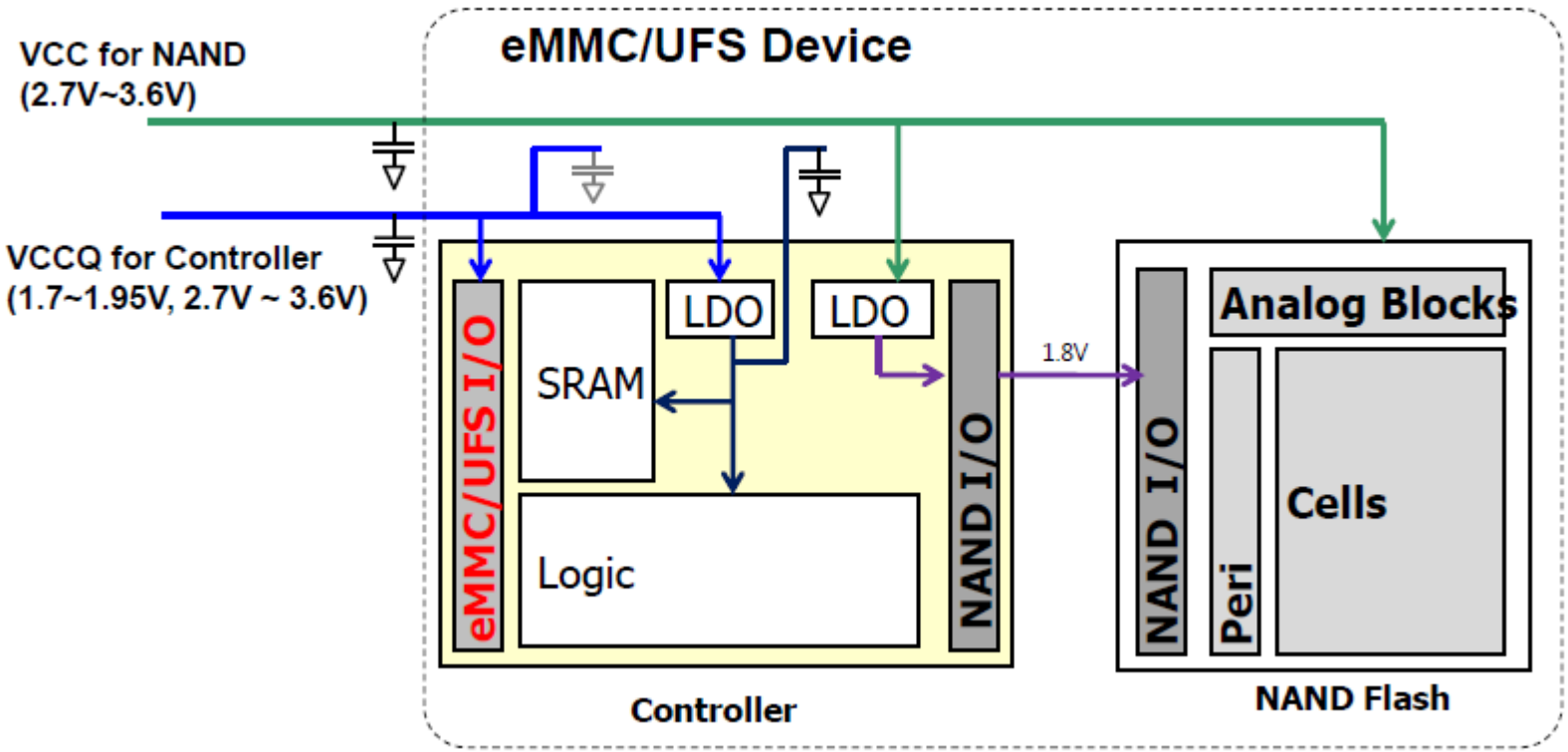




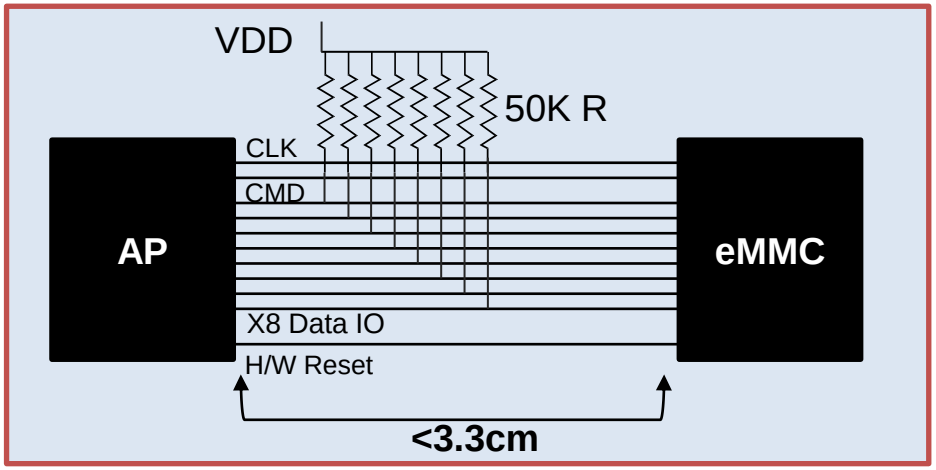
UFS position in Mipi Systems

Simplified eMMC/UFS HW 구조

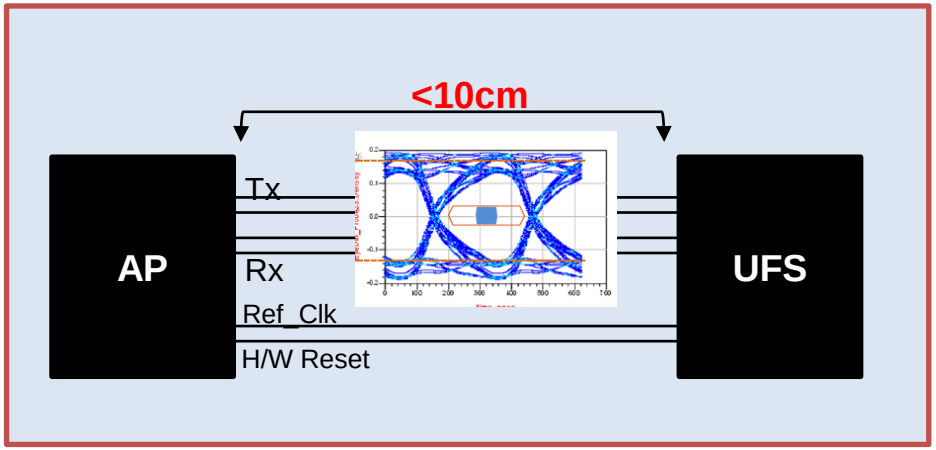
- **Power : Power for NAND Flash, Power for Controller**



UFS : Simple PCB routing and cost save



eMMC PCB Design Connection Guide



UFS PCB Design Connection Guide

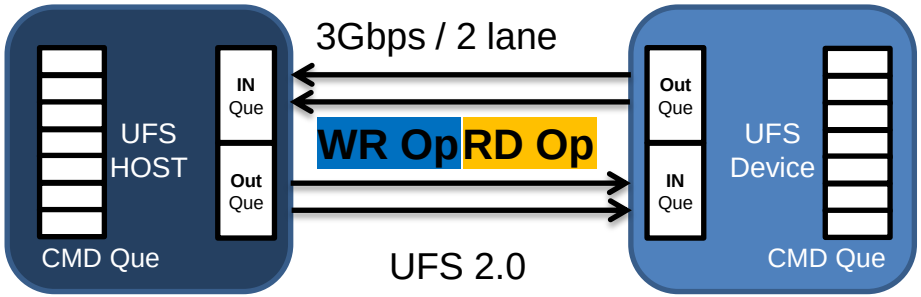
[Table 2] 153 FBGA Ball Information

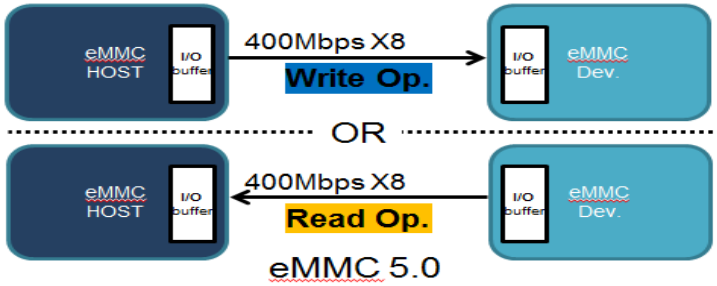
Name	Type	Description
VCC	Supply	Supply voltage for the memory devices
VCCQ2	Supply	Supply voltage used typically for the PHY interface and the memory controller and any other internal low voltage block
VDDiQ	Input	Input terminal to provided bypass capacitor for VCCQ internal regulator typically related to the memory controller
VDDiQ2	Input	Input terminal to provide bypass capacitor for VCCQ2 internal regulator, typically related to memory IF
VDDi	Input	Input terminal to provide bypass capacitor for VCC internal regulator
VSS	Supply	Ground
RST_n	Input	Input hardware reset signal. This is an active low signal
REF_CLK	Input	Input reference clock. When not active, this signal shall be pull-down or driven low by the host SoC.
RXDP0	Input	Downstream data lane: differential input signals into UFS device from the host
RXDN0		
TXDP0	Output	Upstream data lane: differential output signals from the UFS device to the host
TXDN0		
NC	-	Not Connected. NC pins can be connected to ground or left floating
RFU	-	Reserved for Future Use. RFU pins must be left floating.
VSF	-	Vendor Specific Function. VSF pins must be left floating. Each vendor is able to use these pins during manufacturing

Functional Comparison for HW Perspective

Item	eMMC 5.0	UFS 2.0
Host I/F Speed	DDR 400Mhz	**3Ghz x2 Lane(6Ghz)**
Host Signal Type	CMOS	LVDS
I/O swing Level	1.8V	240mV
Comm. Type	Half Duplex	**Full Duplex**
I/O Error Detection	$CRC16_{/512Byte}$	$CRC16_{/272Byte}$
Buffer Control	Busy signal	Unipro support, RTT

- **Major Improvements : Support High B/W and sophisticated I/O Error Handling scheme**
- **Comparison of Communication type.**



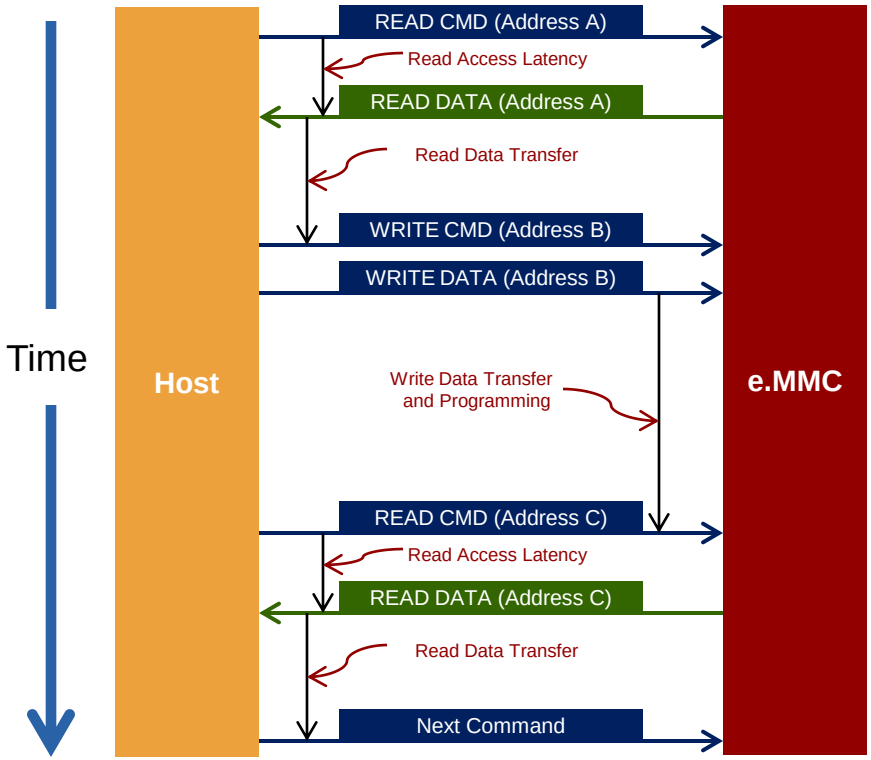


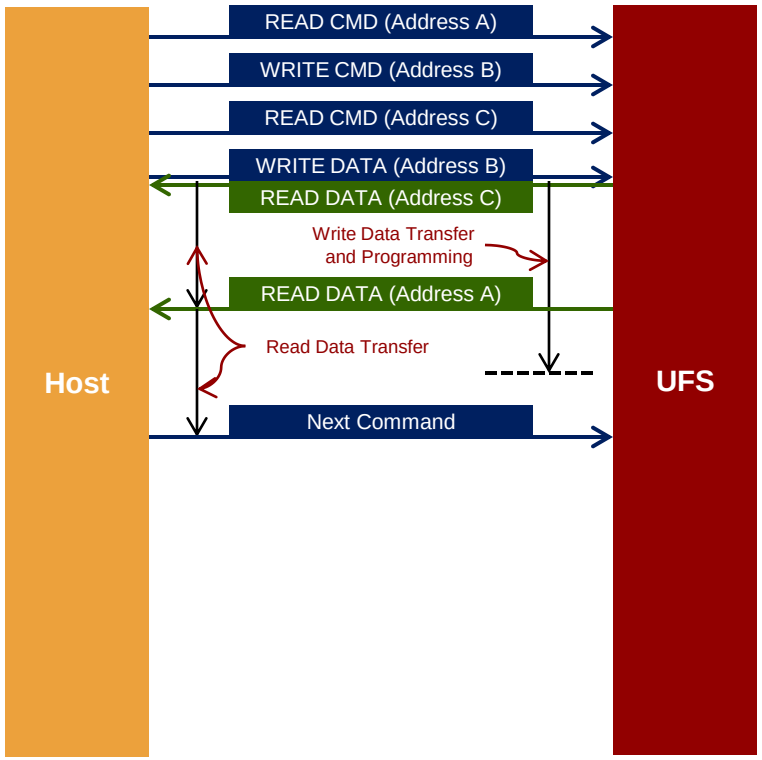
Functional Comparison for SW Perspective

Item	eMMC 5.0	UFS 2.0
Sector Size	512 Byte	4096 Byte (RPMB 512Byte)
RPMB	O	O
#Lun	4	8
Boot Partition	O	O
Fast Boot	O	O
Command Queue	X	O
Concurrent Ops.	X	O
Secure Trim/Erase	O	O
Other eMMC features.	O	O
Command Protocol	eMMC	SCSI

◆ **UFS SW function covers all of eMMC SW features.**

Command Queue



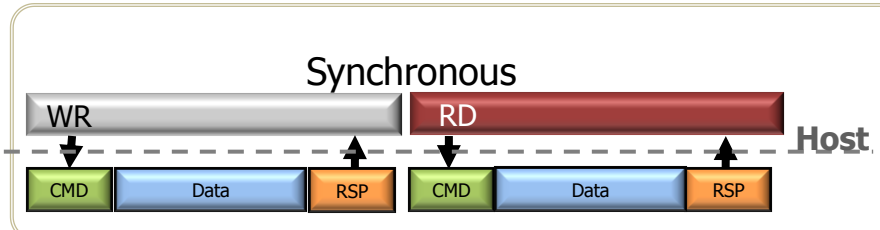


- e.MMC
  - Single-threaded operational model
  - Half-duplex data transfer
  - Must wait for a command execution to complete before issuing the next command
- UFS
  - Supports concurrent operations, command queuing , out-of-order execution
  - Full-duplex data transfer

Read while write

- **Read While Write**
  - **UFS gives you better user experience with low latency and better throughput**

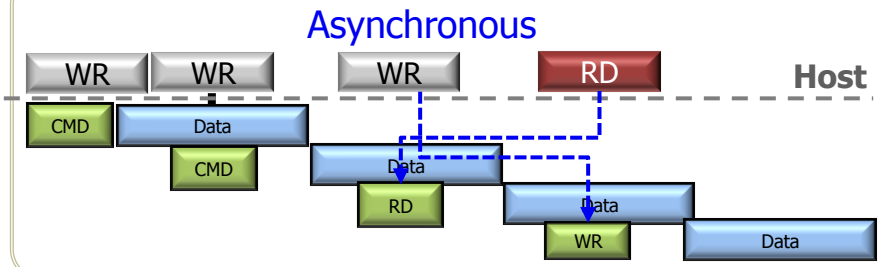
eMMC

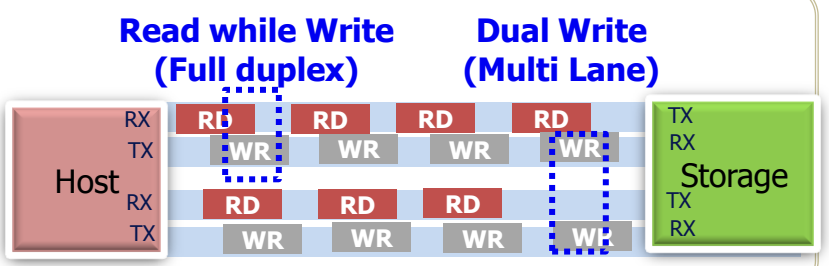


Command Handshaking

Channel Configuration

UFS

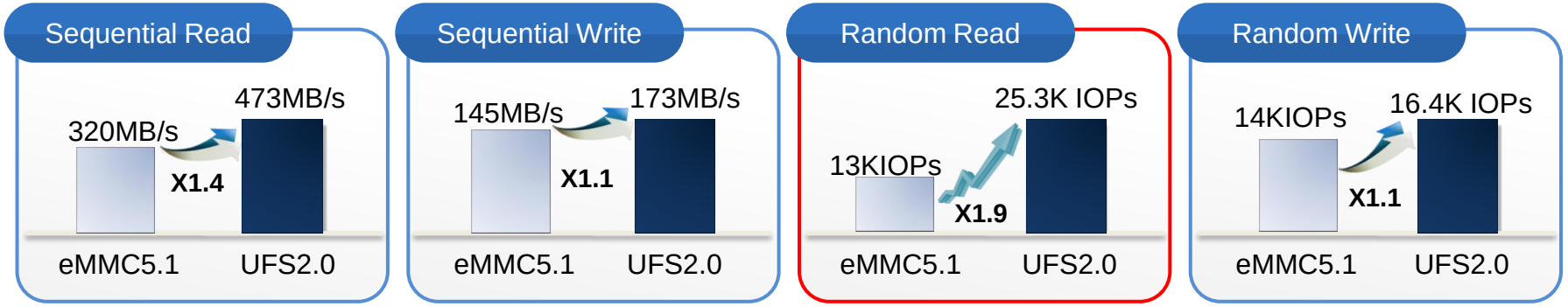


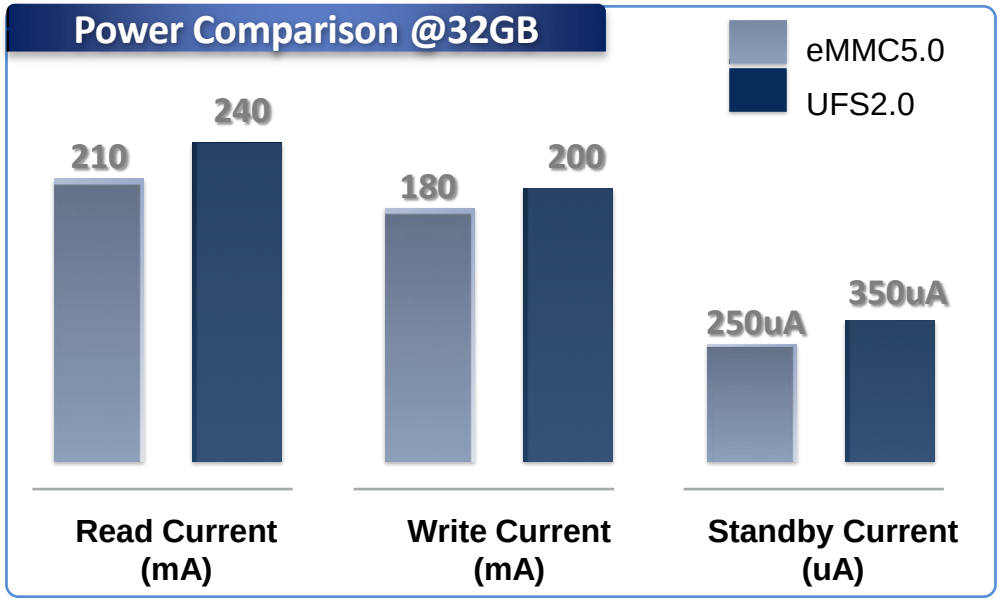


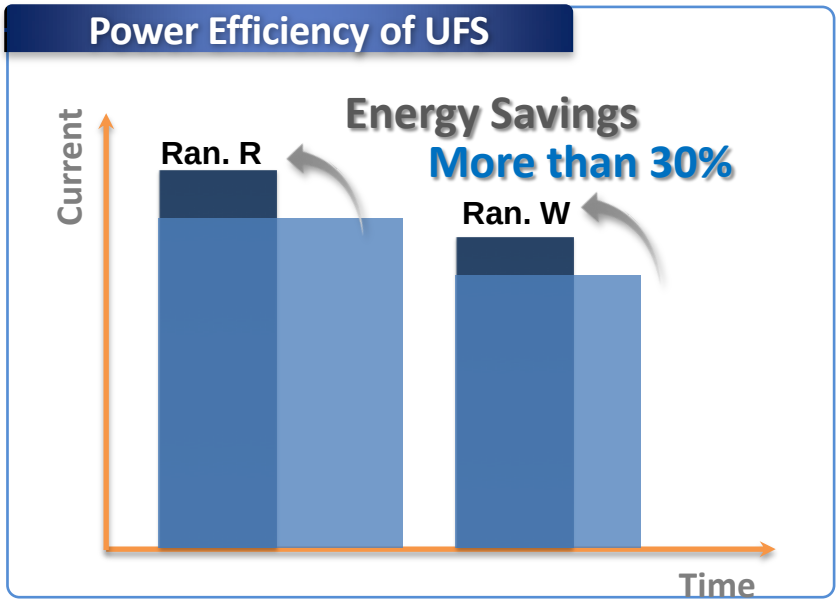
Low Latency for Responsive (Out of order execution)

Better throughput (Simultaneous read and write)

Performance / Power

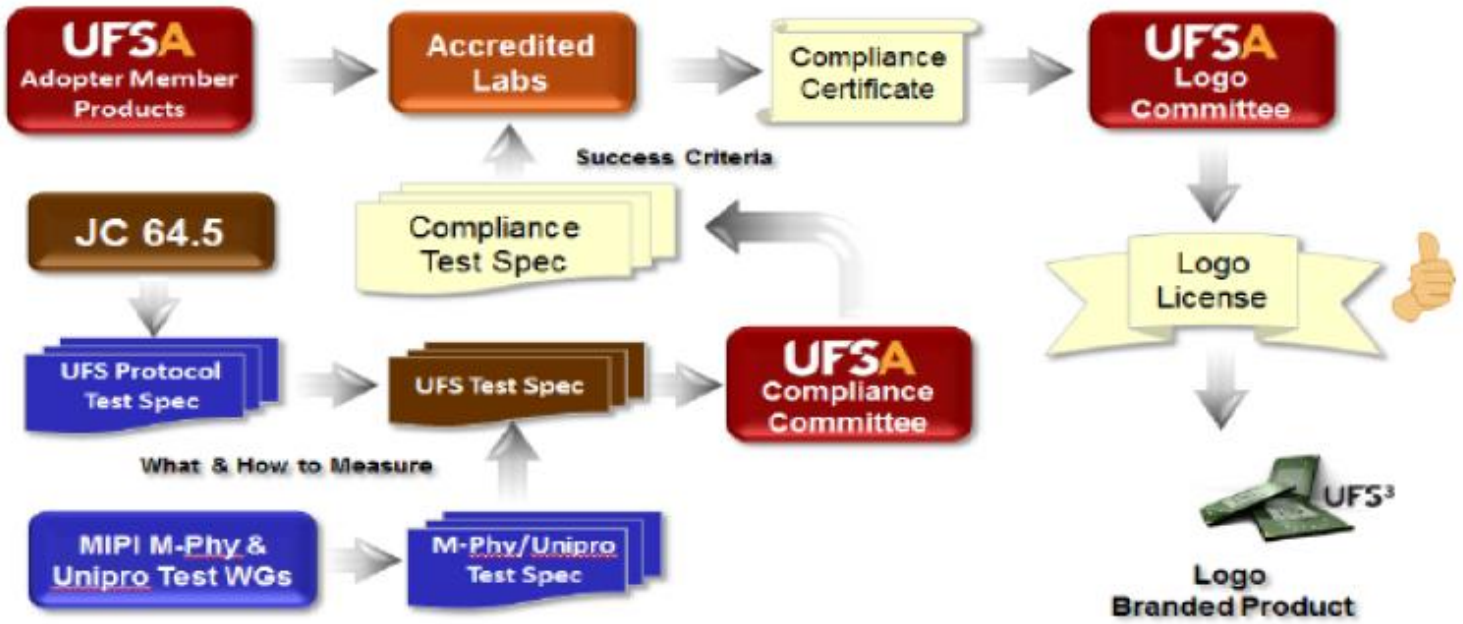






UFS M-PHY Compliance Test Suite

- Serial Interface Compliance Test Suite→ SATA, PCIe, M-PHY 모두 비슷한 인증 과정 적용
- Device 적용 환경에 따른 Compliance Test 환경 다양하게 Set-up 정의



응용기술 Validation list

NO	Item	상세
1	Power integrity	Power supply(VCC/VCCQ2), Power up ramp
2	Signal integrity	Eye Opening, Jitter, REF CLK
3	Functions	Booting, Reset, Sleep
4	Board Design guide	4.7uF+0.22uF(VCC), 2.2uF+0.22uF(VCCQ2)

2015 October eStorage Lineup Update

October 2015

	Available	2015 Q4	2016 Q1	2016 Q2	2016 Q3
UFS		• PKG : 11.5x13x1.2 • UFS2.0 G32L	256GB		
	128GB				
	64GB				
	32GB				
eMMC (MLC)	128GB			• PKG : 11.5x13x1.2	128GB
	64GB			• PKG : 11.5x13x1.0	64GB
	32GB				32GB
	16GB			• PKG : 11.5x13x0.8	16GB
	8GB				
	4GB				
eMMC (TLC)	128GB			128GB	• PKG : 11.5x13x1.2 • eMMC 5.1
	64GB			64GB	• PKG : 11.5x13x1.0 • eMMC 5.1
	32GB				
	16GB				
	8GB				

ES ▽ CS ▽

16nm

1Znm

V3

Thank You!